IEEE

Circuits and Systems

MAGAZINE

Volume 1, Number 2, Second Quarter 2001 ISSN 1531-636X

Filter Banks in Digital Communications

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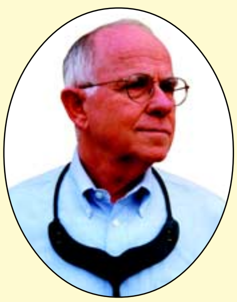

A Microphone Array for Hearing Aids

26

Calls for Papers and Participation

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ICECS'01

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The Westin Dragonara Resort, Malta

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Conference Secretariat:
Eventra Ltd., eventra@co.inet.fi
Pietarinkatu 11 B 40
FIN-00140 Helsinki, Finland
Tel. +358 9 6926 949
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Secretary General:
Timo Veijola, ecctd01@hut.fi
Helsinki University of Technology
P.O. Box 3000, FIN-02015 HUT, Finland
Tel. +358 9 451 2293
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. . . continued on Page 44

IEEE Circuits and Systems MAGAZINE

Volume 1, Number 2, Second Quarter 2001

4 Filter Banks in Digital Communications

by P. P. Vaidyanathan

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26 A Microphone Array for Hearing Aids

by Bernard Widrow

. . . This method enables the design of highly-directive-hearing instruments which are comfortable, inconspicuous, and convenient to use. The array provides the user with a dramatic improvement in speech perception over existing hearing aid designs, particularly in the presence of background noise, reverberation, and feedback.

IEEE Circuits and Systems Magazine (ISSN 1531–636X) is published quarterly by the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY, 10016–5997. Responsibility for the contents rests upon the authors and not upon the IEEE, the Society, or its members. IEEE Service Center (for orders, subscriptions, address changes): 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331. Telephone: +1 732 981 0060, +1 800 678 4333. Individual copies: IEEE members $10.00 (first copy only), nonmembers $20.00 per copy; $7.00 per member per year (included in Society fee) for each member of the IEEE Circuits and Systems Society. Subscription rates available upon request. Periodicals postage paid at New York, NY, and at additional mailing offices. **Postmaster**: Send address changes to IEEE Circuits and Systems Magazine, IEEE Operations Center, 445 Hoes Lane, Piscataway, NJ, 08855.

Printed in U.S.A.

IEEE **Circuits and Systems** MAGAZINE

Frequency of Publication

Quarterly

Magazine Deadlines

Final materials for the *CAS Magazine* must be received by the Editor on the following dates:

Issue	Due Date
First Quarter	February 1
Second Quarter	May 1
Third Quarter	August 1
Fourth Quarter	November 1

Columns and Departments

3 **From the Editor**
by Michael K. Sain

33 **Transactions**
Guillemin-Cauer Award
Darlington Award
Outstanding Young Author
CSVT Best Paper
CAD Best Paper
VLSI Best Paper
VLSI SLIP Special Issue—Call for Papers

36 **Technical Committees**
Nanoelectronics and Gigascale Systems
by Chung-Yu Wu

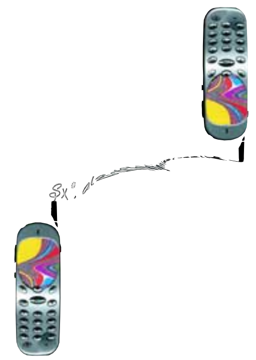
39 **Meetings**
ISCAS 2001 Report
by Chung-Yu Wu and Michael K. Sain

40 **Society**
Swamy Assumes Publications Post
Free Student Membership Promotion
Trajkovic Joins Board
CASS Awards
Van Valkenburg
Technical Achievement
Education
Meritorious Service
Industrial Pioneer
Chapter-of-the-Year
President Names Divisions

41 **The 'Umble Ohm**
by Shlomo Karni

42 **Recognitions**
2001 CASS Fellows

44 **Calls for Papers and Participation**
See also inside front cover and back cover.



Coming next issue:
Chaos in Cryptography.

Scope: A publication of the IEEE Circuits and Systems Society, *IEEE Circuits and Systems Magazine* publishes articles presenting novel results, special insights, or survey and tutorial treatments on all topics having to do with the theory, analysis, design (computer aided design), and practical implementation of circuits, and the application of circuit theoretic techniques to systems and to signal processing. The coverage of this field includes the spectrum of activities from, and including, basic scientific theory to industrial applications. **Submission of Manuscripts:** Manuscripts should be in English and may be submitted electronically in pdf format to the publications coordinator at jordan@medugorje.ee.nd.edu. They should be double-spaced, 12 point font, and not exceed 20 pages including figures. An IEEE copyright form should be included with the submission. **Style Considerations:** 1) articles should be readable by the entire CAS membership; 2) average articles will be about ten published pages in length; 3) articles should include efforts to communicate by graphs, diagrams, and pictures—many authors have begun to make effective use of color, as may be seen in back issues of the *Newsletter*, available at www.nd.edu/~stjoseph/newscas/; 4) equations should be used sparingly.

From the Editor

Michael K. Sain
Editor-in-Chief, *IEEE Circuits and Systems Magazine*

A Circuits and Systems Carrousel

Now that *IEEE Circuits and Systems Magazine* has completed its second issue, we are able to perceive the skeleton begin to form, and we want to say a few words about the flesh which in due course will fill out the body.

According to the dictionary, the word carrousel has a first meaning of a friendly contest. Here one may imagine several groups which are vying for a prize. The prize is envisioned as the center of activity, with the groups arranged around the center. It is a unifying image, with the groups becoming closer to each other as they move toward the center. The second meaning of carrousel is that of a merry-go-round, which has multiple interpretations. One pleasant associated image is that of children riding horses mounted on a turning platform. One less pleasant meaning is that of a humdrum, repetitive existence, not necessarily desirable at all.

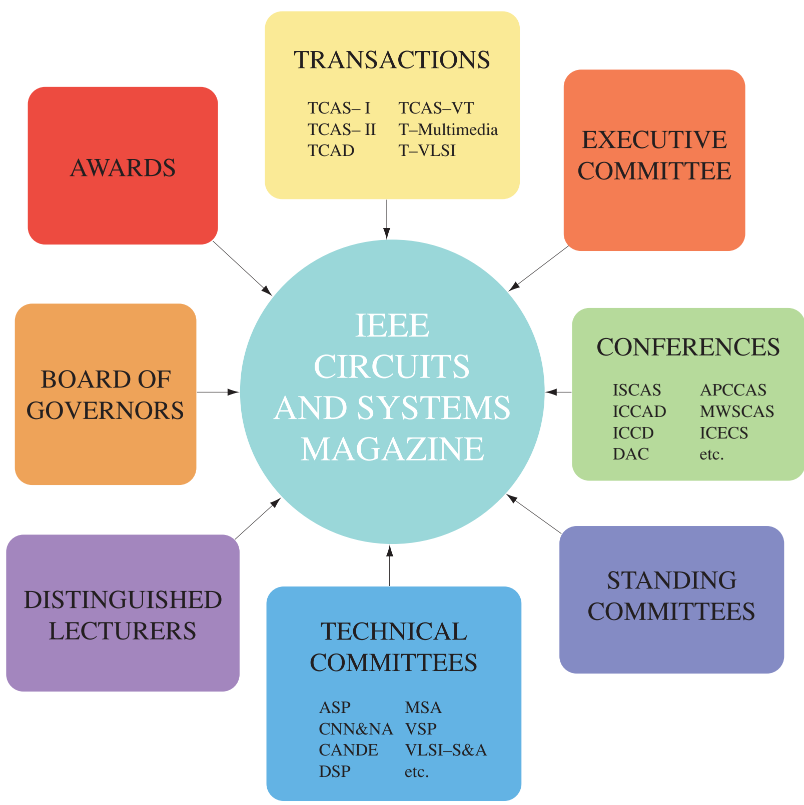
Even though the second meaning is the more commonly known, we choose the first meaning, because it is a good fit for what the Circuits and Systems Society has in mind for this magazine. Indeed, in the figure on this page, one may see a Circuits and Systems Society Carrousel, with some of the constituent groups represented around the magazine as a focus. In this simplified diagram, it was not possible to show every one of the Society entities; but these are indicative.

A major goal of the *IEEE Circuits and Systems Magazine* is to be a sort of lens at the center of the Society, a lens through which the activities of the various constituencies can be magnified and focussed for the general membership. Clearly, this involves the publication of up-to-date articles to reach our broad audience. We are already working hard on this aspect, but there is a limit on the amount of space available, and so we will have to rotate through the topics of interest. So if your topic has not yet appeared, please be patient and do not hesitate to send us your suggestions.

Beyond the articles, which are certainly the most obvious of the contents, we have the goal of factoring in the developments in our Divisions—described elsewhere in this issue. These would include our technical committees, our transactions, our meetings and workshops, and our regional subsocieties. We have begun this process in our Columns and Departments pages as part of issue one, and we continue it as part of this issue two. Additional plans are being laid for issue three.

Fleshing out the body of the carrousel will of course require horses and riders. If all those who can, do contribute, it will grow into a principal attraction on the midway.

Anyone want a ticket?



Filter Banks in Digital Communications

by P. P. Vaidyanathan

Abstract—*Digital signal processing has played a key role in the development of telecommunication systems over the last two decades. In recent years digital filter banks have been occupying an increasingly important role in both wireless and wireline communication systems. In this paper we review some of these applications of filter banks with special emphasis on discrete multitone modulation which has had an impact on high speed data communication over the twisted pair telephone line. We also review filter bank precoders which have been shown to be important for channel equalization applications.*[1]

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Introduction

Efficient and successful communication of messages via imperfect channels is one of the major triumphs of information technology today. With more and more users desiring to share communication channels, the importance of clever exploitation of the bandwidth becomes paramount. For example telephone lines (twisted-pair channels) which were originally intended to carry speech signals (about 4 kHz bandwidth) are today used to carry several megabits of data per second. This has been possible because of efficient use of high frequency regions which suffer from a great deal of line attenuation and noise. As a result of these developments the twisted pair telephone line, which reaches nearly every home and office in the western world, can today handle high speed internet traffic as exemplified by popular services such as the DSL (digital subscriber loop), ADSL, and so forth. As someone pointed out, *twisted pair copper lines are buried but not dead*, thanks to advanced signal processing technology!

Communication channels can be wireless or wireline channels, or a combination of both. In any case they introduce linear and nonlinear distortions, random noise components, and deterministic interference. The transmission of information with high rate and reliability under such unfavorable conditions has been possible because of fundamental contributions from many disciplines such as information theory, signal processing, linear system theory, and mathematics.

The role of digital signal processing in communication systems has been quite significant [1, 2, 3]. In this paper we emphasize some of these, especially the role of filter banks. The aim here is to give an overview of filter banks as applied to digital communication systems. Filter banks were originally proposed for application in speech compression more than 25 years ago (see references in [4]). Today they are used for the compression of image, video, and audio signals, and the story of their success can be found in many references. More recently filter banks have been used in digital communication systems in many forms. Some of these include perfect digital transmultiplexing [5, 6], filterbank precoding for channel equalization [7, 8], equalization with fractionally spaced sampling [9], and discrete multitone modulation [2, 10, 11]. Filter banks have been used in high speed DSL services for internet traffic [3]. They have also been considered for blind equalization in wireless channels [12, 13].

[1] Work supported in parts by the NSF grant MIP 0703755 and ONR grant N00014-99-1-1002.

The Noisy Channel

In this paper we model the communication channel as a linear time invariant system with transfer function $C(z)$ followed by an additive Gaussian noise source $e(n)$ as shown in Fig. 1. In a digital communication system each sample $x(n)$ comes from a fixed finite set of values. This set of values is called a constellation, some standard examples being PAM and QAM constellations explained in Fig. 2. If each symbol $x(n)$ is a b-bit number and there are f_s symbols per second, then the **bit rate** is $\mathcal{R} = bf_s$ bits per second. For example if $f_s = 1$ MHz and $b = 4$ then $\mathcal{R} = 4$ megabits per second (Mbps).

The received signal $y(n)$ is a noisy and distorted version of $x(n)$. The detector at the receiver has to guess the value of $x(n)$ based on $y(n)$. The estimated value $\hat{x}(n)$ belongs to the same

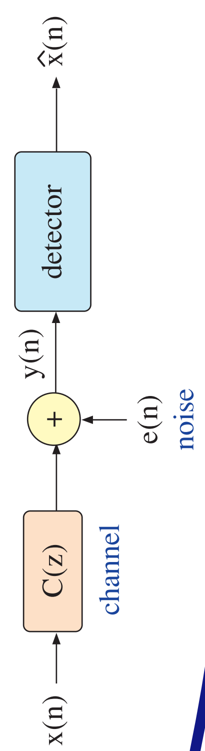
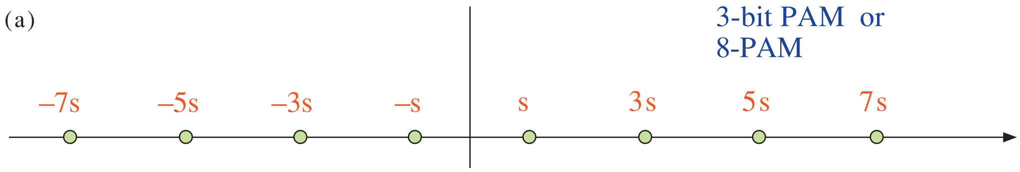


Figure 1. A simple model for a digital communication system. Here a sequence of symbols x(n) is transmitted through a channel with transfer function C(z) and additive noise e(n).

(a)



(b)

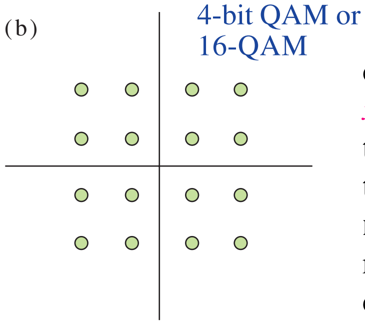


Figure 2. (a) For the case of Pulse Amplitude Modulation (PAM), the sample $x(n)$ is a quantized real number as demonstrated in part (a) for 3-bit PAM (also called 8-PAM). (b) For the case of Quadrature Amplitude Modulation (QAM) $x(n)$ can be regarded as a compex number, taking one of 2^b possible values from a rectangular constellation as demonstrated in part (b) for $b = 4$ bits (called 16-QAM). More efficient constellations exist [14]. The distance between the constellation words (e.g., s in part (a)) can be controlled to control the transmitted power.

constellation that $x(n)$ came from. If $x(n) = \hat{x}(n)$ there is no error; otherwise the detection is erroneous. In practice there is a nonzero **probability of error** $\mathcal{P}_e$ in this detection because of the noise $e(n)$ and the intersymbol interference caused by the channel $C(z)$. The acceptable value of $\mathcal{P}_e$ depends on application. For example it is in the range 10^{-7} to 10^{-9} for DSL applications; for digital speech with mobile phone quality, larger $\mathcal{P}_e$ is acceptable whereas for deep space communication, $\mathcal{P}_e$ has to be quite a bit smaller.

The model shown in Fig. 1 does not work in all situations. For example, mobile phone channels are time varying because of vehicular movement, and a single $C(z)$ cannot be used to represent them successfully. However a number of practical channels (e.g., the wireline telephone channel) can be approximated by this. A second remark is that the figure implicitly uses discrete time notations. In practice, the sequence $x(n)$ is converted into a continuous time pulse train $\sum_n x(n)p(t-nT)$ before imposing it on the channel. The output of the channel is sampled and digitized to obtain $y(n)$. These details are not shown in the figure. It should be understood that $C(z)$ and $e(n)$ are the effective discrete time equivalents of the actual channel parameters.

Power Allocation and Water-Filling Strategy

The transmitted signal **power** P is proportional to the mean square value of $x(n)$. Assume that $x(n)$ is a wide sense stationary random process [14]. Then the power is the integral of the power spectrum $S_{xx}(e^{j\omega})$, that is, $P = \int_0^{2\pi} S_{xx}(e^{j\omega})d\omega/2\pi$. For a given channel the average probability of error $\mathcal{P}_e$ at the receiver depends on the transmitted power P, and the bit rate $\mathcal{R}$. We can decrease the error probability by transmitting more power. For fixed power, the error probability increases with bit rate $\mathcal{R}$.

Note that the power spectrum of $x(n)$ tells us how its **power is distributed** in frequency. By carefully shaping it, we can increase the achievable rate (for fixed error probability and transmitted power). The idea is to "pour" more power in the regions where the channel gain is large and noise spectrum is small. This can be pursued in a mathematically rigorous way using fundamentals from information theory [14].

If the transfer function of the channel is known, then the detector can equalize it by using the filter $1/C(z)$. This is called the ideal equalizer. It is also known as the **zero-forcing** equalizer for reasons explained in [14]. In practice $1/C(z)$ can be approximated with a stable (possibly FIR) filter. As seen from Fig. 3, the effective noise $q(n)$ seen by the receiver is $e(n)$ filtered through $1/C(z)$. This has the effective noise power spectrum

$$S_{qq}(e^{j\omega}) \triangleq \frac{S_{ee}(e^{j\omega})}{|C(e^{j\omega})|^2}. \quad (1)$$

This ratio summarizes the channel completely for the purpose under discussion. If $C(z)$ has zeros close to the

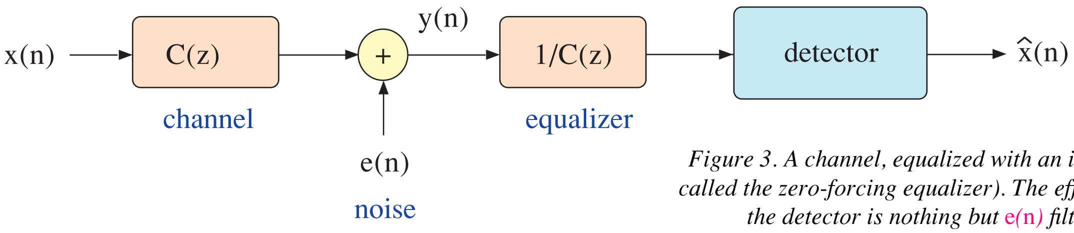


Figure 3. A channel, equalized with an ideal equalizer $1/C(z)$ (also called the zero-forcing equalizer). The effective noise $q(n)$ as seen by the detector is nothing but $e(n)$ filtered through $1/C(z)$.

unit circle, then $1/C(z)$ has poles near the unit circle and the noise gain can be large. In frequency regions where the ratio $S_{qq}(e^{j\omega})$ is small, we should allocate more power. In fact the optimal power distribution $S_{xx}(e^{j\omega})$ can be described precisely with the help of Fig. 4. This figure says that

$$S_{xx}(e^{j\omega}) = \begin{cases} \lambda - S_{qq}(e^{j\omega}) & \text{when} \geq 0 \\ 0 & \text{otherwise} \end{cases} \tag{2}$$

where λ is a constant. That is, the transmitted power at a frequency should be equal to the gap between λ and $S_{qq}(e^{j\omega})$. Notice that in regions where the channel is "too bad" $(S_{qq}(e^{j\omega}) > \lambda)$ we transmit no power at all. If we imagine a bowl with its bottom shaped like $S_{qq}(e^{j\omega})$, then $S_{xx}(e^{j\omega})$ is the height of water filling the bowl, with λ denoting the uniform water level everywhere. This is a classic result on power allocation, and is called the **water filling** rule [14]. It is clear that the area under $S_{xx}(e^{j\omega})$ (total power) increases with choice of λ. The choice of λ therefore depends on the total available power P.

For fixed total power P and fixed channel, the **capacity** $\mathcal{C}$ is the maximum rate at which information can be transmitted with arbitrarily small error probability. This should not be confused with the actual bit rate $\mathcal{R}$ with nonzero error probality $\mathcal{P}_e$. Evidently if $\mathcal{P}_e$ is allowed to be large enough then $\mathcal{R}$ can be made larger than the capacity $\mathcal{C}$. In situations where $\mathcal{P}_e$ is required to be reasonably small, $\mathcal{C}$ can be regarded as a useful bound on acheivable rate $\mathcal{R}$.

How do we shape the power spectrum $S_{xx}(e^{j\omega})$ to satisfy the water-filling type of power allocation? This is tricky because we do not have a great deal of freedom to shape things, especially if $x(n)$ is user generated data! For example $x(n)$ could be binary data or data from a PAM or QAM constellation, and might behave like an iid (independent identically distributed) sequence

Filter Banks in Digital Communications

Filter Banks in Digital Communications

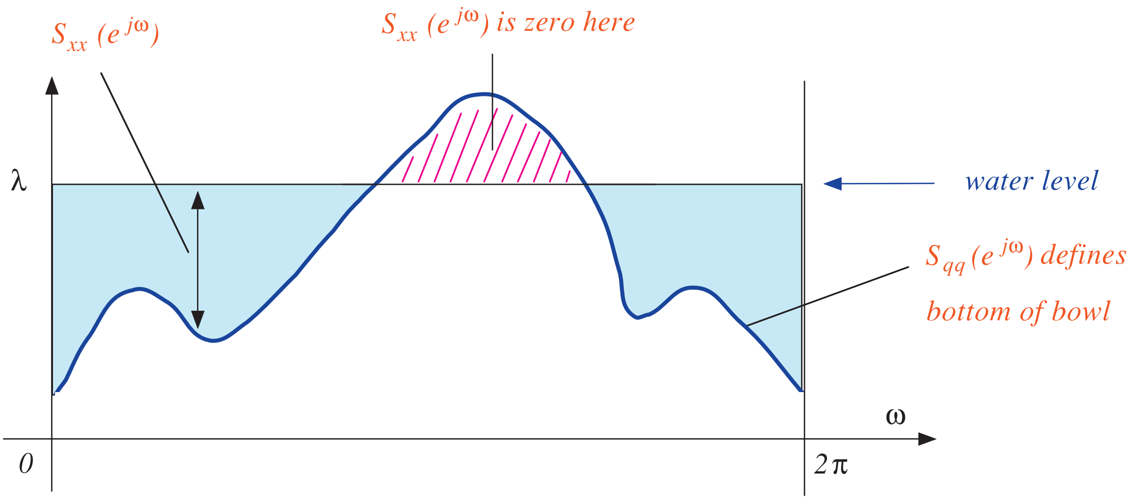


Figure 4. Relation between the input power spectrum $S_{xx}(e^{j\omega})$ and the effective noise power spectrum $S_{qq}(e^{j\omega})$ to achieve maximum rate for fixed total power. This is called the water filling rule.

Filter Banks in Digital Communications

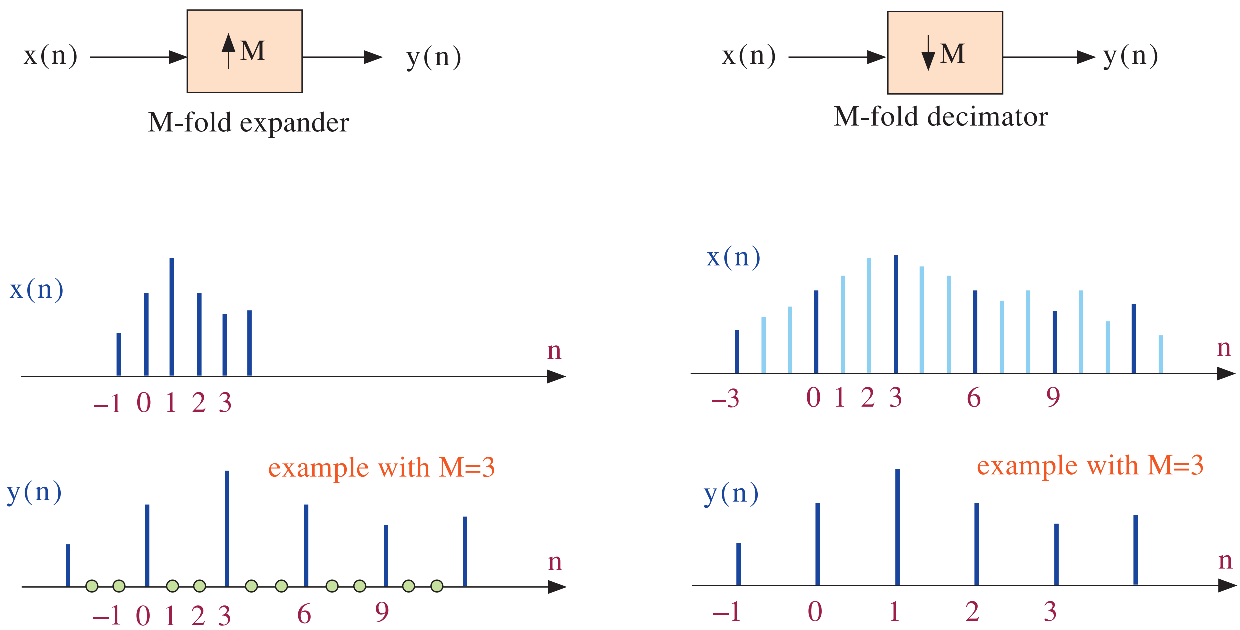


Figure 5. The M*-fold expander merely inserts* M – *1 zeros between adjacent samples, as demonstrated in the figure for* M = *3. The* M*-fold decimator has input-output relation* y(n) = x(Mn)*. Thus, only a subset of input samples are retained. This is demonstrated in the figure for* M = *3. Note that the samples automatically get renumbered so that* y(*1*) = x(M)*,* y(*2*) = x(2M) *and so forth.*

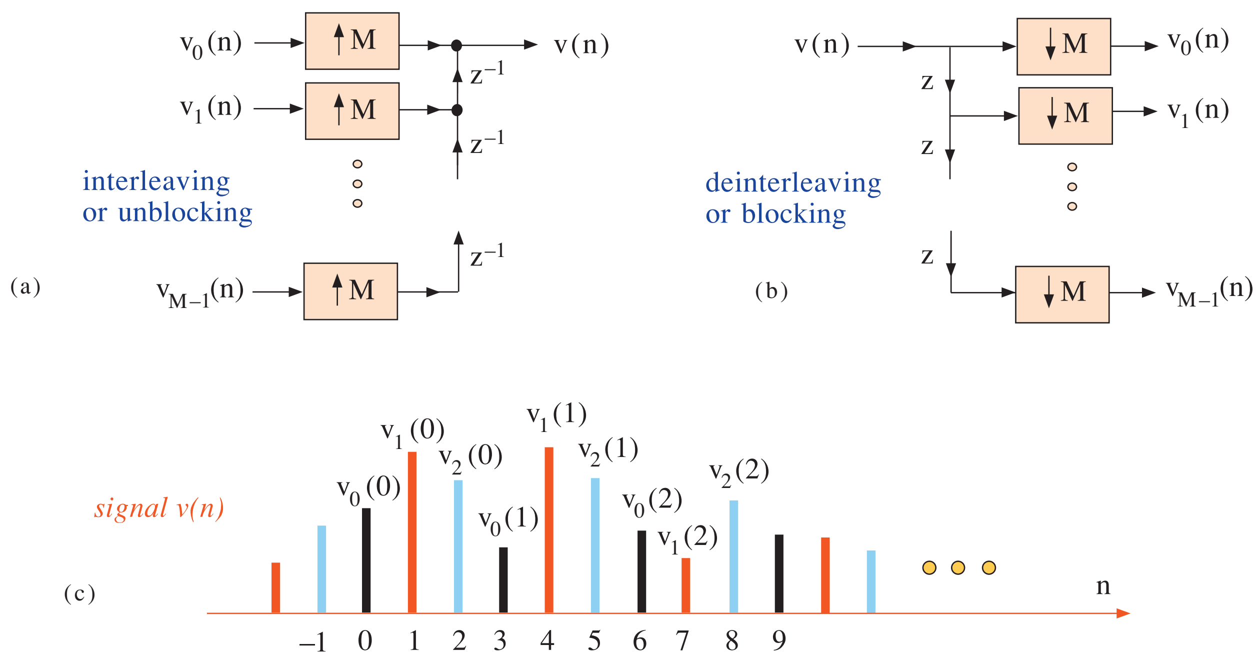


Figure 6. (a), (b) The operations of interleaving and deinterleaving using multirate building block notation. (c) Demonstration for M = *3. The interleaving operation is also called unblocking. Similarly deinterleaving is also called blocking.*

with a practically flat power spectrum. A clever way to approximate optimal power allocation would be to divide the channel bandwidth into several subbands and transmit in each subband channel separately [15, 16]. This already suggests a resemblance to frequency division multiplexing but the main difference now is that the different subband channels carry different parts of a single input stream. How this is actually accomplished will be explained in the section *Discrete Multitone Modulation (DMT)*.

Decimators, Expanders, and Multiplexers

Before proceeding further we review a few standard building blocks and terminology used in multirate signal processing. Most of the details can be found in [17]. The building blocks $\uparrow M$ and $\downarrow M$, shown in Fig. 5, are called the expander and decimator respectively. Their operation is explained in the figure caption.

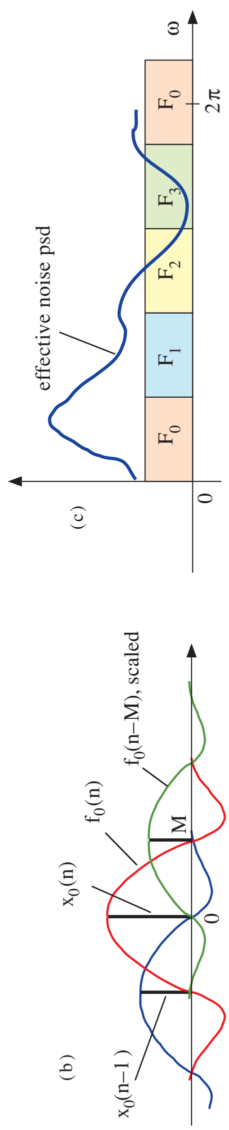
Two standard operations called "blocking" and "interleaving" often arise in communication systems that use filter banks. It is sometimes convenient to explain these using multirate building blocks. These are shown in Figs. 6(a) and 6(b). The connection between the signal $v(n)$ and the "blocked components" $v_k(n)$ is indicated in Fig. 6(c) using the example of $M = 3$. It is clear that we can regard $v(n)$ as a **time-domain multiplexed** or **TDM** version of the individual signals $v_k(n)$. The components $v_k(n)$ are also called the **polyphase** components of $v(n)$ with respect to M [17].

The Digital Transmultiplexer

Our next step would be to describe the operation of a filter bank structure called the transmultiplexer [18, 5, 17]. It was originally intended to convert data between time division multiplexed (TDM) format and frequency division multiplexed (FDM) format. Figure 7(a) shows a schematic of this in all-discrete language. Here $F_k(z)$ are called transmitting filters or interpolation filters. The kth transmitting filter has output

$$u_k(n) = \sum_{i=-\infty}^{\infty} x_k(i) f_k(n - iM) . \quad (3)$$

Figure 7(b) demonstrates how this construction is done for the 0th filter $F_0(z)$, assumed to be lowpass. Essentially we draw one copy of the impulse response sequence $f_0(\cdot)$ around every sample of $x_0(n)$ (separated by M) and add them up. Thus $u_k(n)$ is an interpolated version of $x_k(n)$ and has M times higher rate. The outputs of the filters $F_1(z), F_2(z)$ and so forth are more complicated waveforms because they are bandpass. The filters $\{F_k(e^{j\omega})\}$ traditionally cover different uniform re-



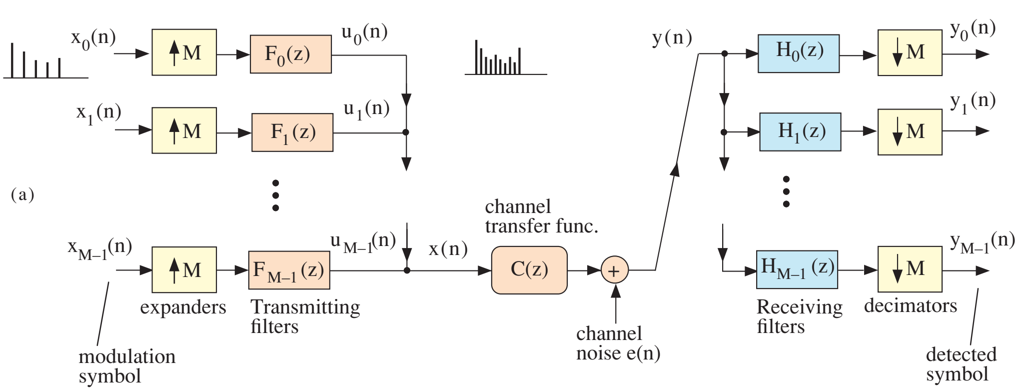
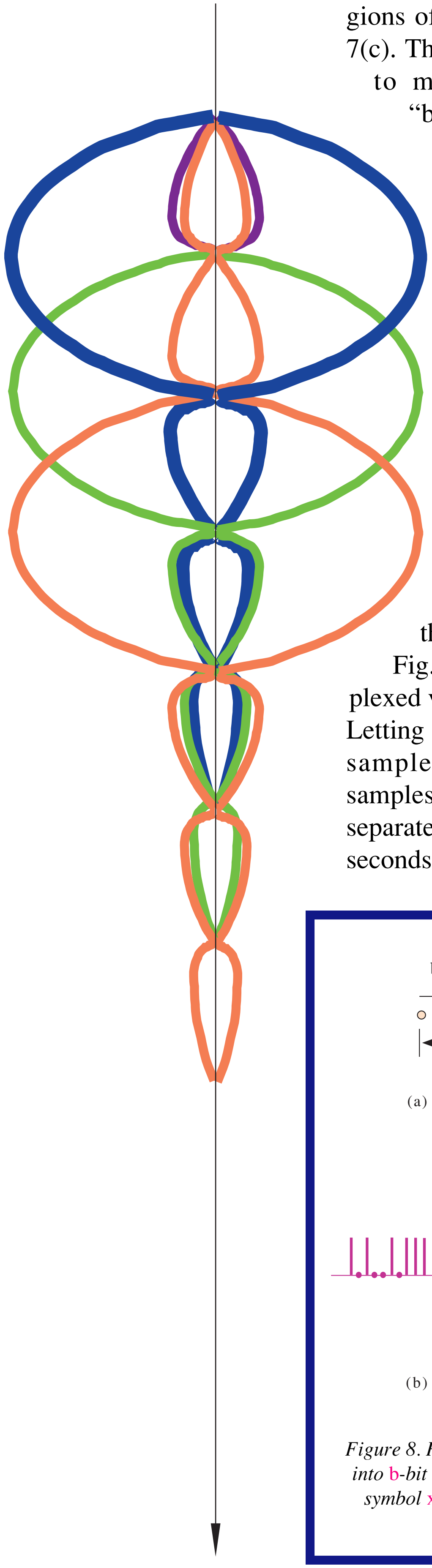


Figure 7. (a) The digital transmultiplexer, (b) operation of the interpolation filter $F_0(z)$, and (c) frequency responses of the transmitting filters (assumed to be ideal infinite order filters). Only the envelope of the samples of $f_0(n)$ are shown in (b).



gions of frequency as shown in Fig. 7(c). The signals $u_k(n)$ are analogous to modulated versions of the "baseband" sequence $x_k(n)$ because the bandwidth is shifted to the passband of $F_k(z)$. These are packed into M adjacent frequency bands (passbands of the filters) and added to obtain the composite signal $x(n)$. With the filters $F_k(z)$ chosen as good bandpass filters, we can regard $x(n)$ as a **frequency division multiplexed** or **FDM** version of the separate signals $x_k(n)$. By contrast, if $F_k(z)$ are just delay elements z^{-k}, then the transmitter part is similar to Fig. 6(a) and $x(n)$ is a time-multiplexed version of the M signals $x_k(n)$. Letting T denote the spacing between samples of $x(n)$, we see that the samples of $x_k(n)$ for any given k are separated by a longer duration of MT seconds.

The receiving filter bank $\{H_k(z)\}$ separates the signal $y(n)$ into the components $y_k(n)$ which are distorted and noisy versions of the symbols $x_k(n)$. The task at this point is to detect the symbols $x_k(n)$ from $y_k(n)$ with acceptable error probability. Thus, even though $x_k(n)$ is interpolated to get $u_k(n)$, it is not necessary to ensure $u_k(Mn) = x_k(n)$; the crucial issue is to make $y_k(n)$ resemble $x_k(n)$.

Discrete Multitone Modulation (DMT)

The transmultiplexer configuration is used in another scheme called **discrete multitone modulation** or DMT. The main difference is in the interpretation of the signals $x(n)$ and $x_k(n)$. To explain this consider Fig. 8(a) which shows the first stage of multitone modulation [15] called the **parsing stage**. Here $s(n)$ represents **binary data** to be transmitted over a channel. This data is divided into nonoverlapping b-bit blocks. The b bits in each block are partitioned into M groups,

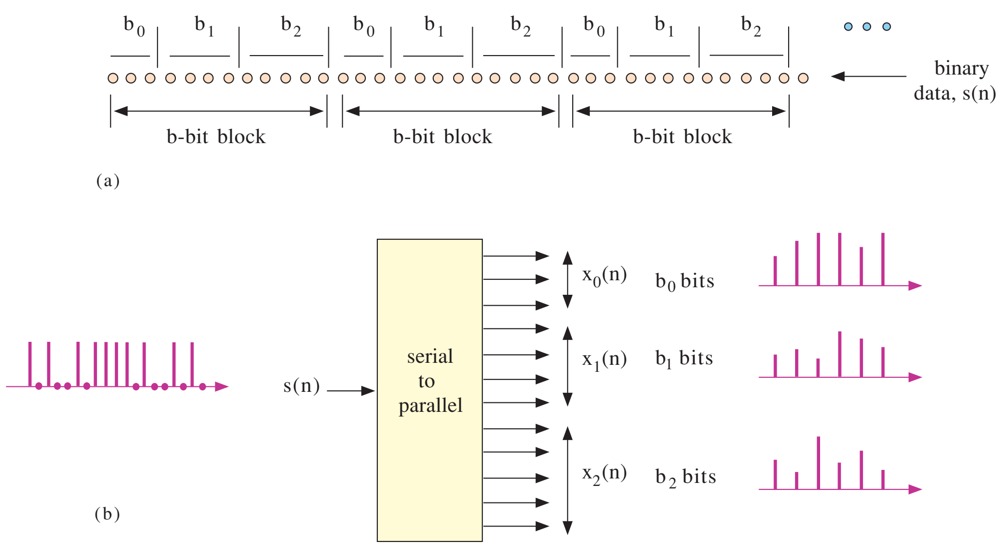


Figure 8. Parsing stage in discrete multitone (DMT) modulation. A binary stream $s(n)$ is subdivided into b-bit blocks and each block is subdivided into M subgroups. The kth subgroup defines a b_k-bit symbol $x_k(n)$. Note that $x_k(n)$ and $x_k(n+1)$ are separated by bT seconds if $s(n)$ and $s(n+1)$ are separated by T seconds.

the kth group being a collection of b_k bits (demonstrated in the figure for $M = 3$). Thus the total number of bits b per block can be expressed as

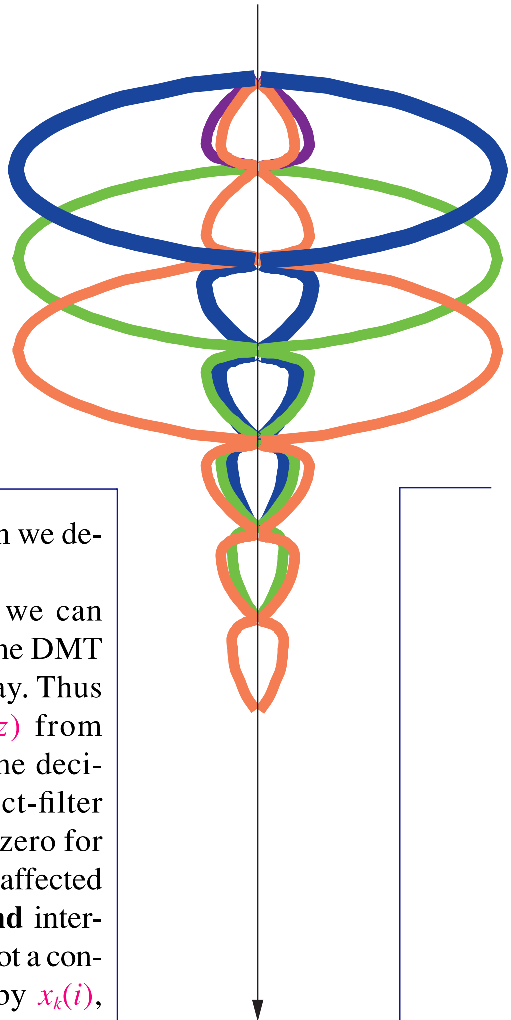
$$b = \sum_{k=0}^{M-1} b_k \quad . \tag{4}$$

The b_k bits in the kth group constitute the kth symbol x_k which can therefore be regarded as a b_k-bit number. For the nth block, this symbol is denoted as $x_k(n)$. This is the **modulation symbol** for the kth band. The collection of symbols $\{x_0(n), x_1(n), \ldots, x_{M-1}(n)\}$ is together referred to as the **DMT symbol**. The sample $x_k(n)$ is typically a PAM or a QAM symbol (Fig. 2). The transmitting filters $f_k(n)$ create the M-fold higher rate signals $u_k(n)$ as before, which are then added to produce the composite signal $x(n)$. In this way, various parts of the original binary message $s(n)$ are packed into different frequency regions allowed by the channel [15, 16].

Notice that for a given constellation, the power can be increased or decreased by scaling the distance between the codewords (e.g., by adjusting s for the PAM constellation in Fig. 2(a)). We therefore have the freedom to allocate different powers for different subband channels. In this way the classical **water-filling rule can be approximated**. For a given transmitted power and probability of error, multitone modulation yields better bit rate than single tone modulation ($M = 1$ case), assuming no channel coding.

Background material on the DMT system and more generally on the use of digital filter banks in communications can be found in [6, 19, 16, 10]. The DMT idea is similar in principle to **subband coding** [4, 20, 17] where a signal $x(n)$ to be quantized is first decomposed into subbands.

Biorthogonality and Perfect DMT Systems



Consider a linear time invariant system with impulse response $h(n)$ and transfer function $H(z)$ sandwiched between an expander and decimator (Fig. 9(a)). It can be shown that this is equivalent to a linear time invariant system with decimated impulse response $g(n) = h(Mn)$. In z-transform notation we denote this as $G(z) = [H(z)]_{\downarrow M}$.

Using this simple idea, we can understand the operation of the DMT system in a very effective way. Thus the transfer function $D_{km}(z)$ from $x_m(\cdot)$ to $y_k(\cdot)$ in Fig. 7(a) is the decimated version of the product-filter $H_k(z)C(z)F_m(z)$. If this is nonzero for $m \neq k$ then the symbol $y_k(n)$ is affected by $x_m(i)$ resulting in **interband** interference. Similarly if $D_{kk}(z)$ is not a constant then $y_k(n)$ is affected by $x_k(i)$, $i \neq n$, due to the filtering effect of $D_{kk}(z)$. This is called **intraband** interference. If interband and intraband interferences are eliminated, the DMT

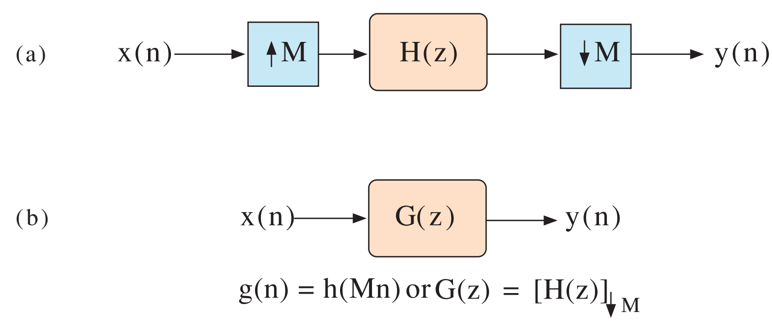


Figure 9. A transfer function H(z) sandwiched between an expander and a decimator is equivalent to another transfer function G(z) with impulse response g(n) = h(Mn).

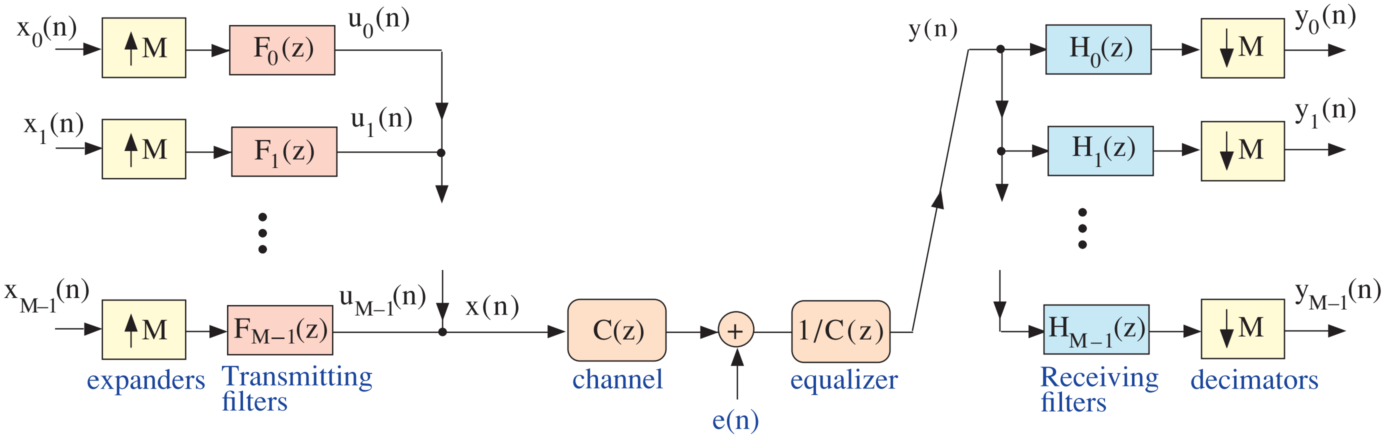


Figure 10. The DMT system with ideal channel equalizer $1/C(z)$. This system has the perfect symbol recovery (PR) property in absence of noise if the filter bank $\{H_k, F_m\}$ is biorthogonal. See text.

system is said to be free from **intersymbol** interference (ISI). If we assume that the filters are ideal nonoverlapping bandpass filters stacked as in Fig. 7(c), then there is no interband interference. Furthermore, suppose that $C(z)$ is completely equalized with the inverse filter $1/C(z)$ as shown in Fig. 10. Then the system is ISI free, and $y_k(n) = x_k(n)$ for all k (in absence of noise), and we have the perfect symbol recovery or **PR** property.

Ideal nonoverlapping filters are of course unrealizable, and good approximations of such filters are expensive. It turns out that perfect symbol recovery can be obtained even with non-

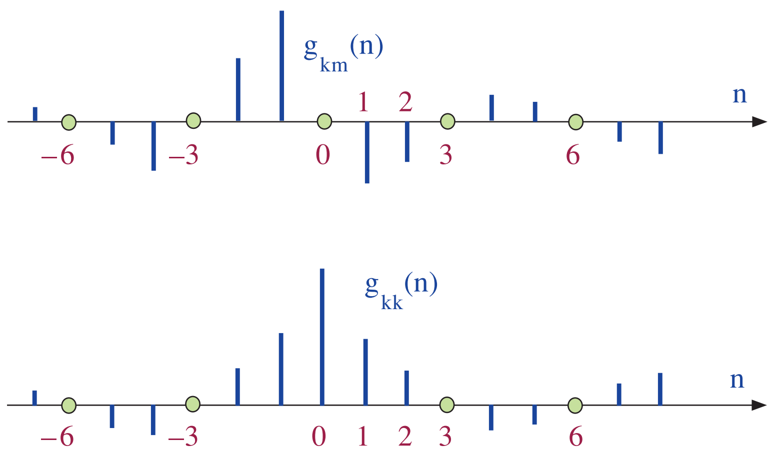


Figure 11. In a biorthogonal transmultiplexer, we have the perfect symbol recovery property in absence of channel distortion $C(z)$ and channel noise $e(n)$. This is achieved by constraining the filters such that the products $G_{km}(z)$ have the Nyquist (M) property. That is, their impulse responses have the zero crossing property at integer multiples of M as demonstrated above for $M = 3$.

ideal filters having overlapping responses. This idea goes back to early work on transmultiplexers [5] and is related to the notion of a biorthogonal filter bank. To explain this, consider what happens when the channel introduces no distortion ($C(z) = 1$). Under this condition we have perfect symbol recovery if and only if the transmitting and receiving filters satisfy the **biorthogonality property** defined as

$$H_k(z)F_m(z)\Big|_{\downarrow M} = \delta(k-m)\,. \qquad (5)$$

This means that the impulse response $g_{km}(n)$ of the product filter $G_{km}(z) \triangleq H_k(z)F_m(z)$ has the **Nyquist(M)** or zero-crossing property

$$g_{km}(Mn) = 0 \qquad (6)$$

for $k \neq m$ and $g_{kk}(Mn) = \delta(n)$ as demonstrated in Fig. 11 for $M = 3$. This condition is readily achieved with careful design of filters. For example, it is possile to design FIR biorthogonal filter banks with almost any filter length.

In this paper we shall make the simplifying assumption that $\{F_m, H_k\}$ is biorthogonal (i.e., Eq. (5) holds) and that the channel transfer function $C(z)$ is equalized by using the inverse filter or zero-forcing equalizer $1/C(z)$ just before entering the bank of filters $\{H_k(z)\}$. In a biorthogonal DMT system with zero-forcing equalizer, the only remaining distortion is due to the channel noise. The received symbol can be written as

$$y_k(n) = x_k(n) + q_k(n) \qquad (7)$$

where $q_k(n)$ is the channel noise filtered through $H_k(z)/C(z)$ and decimated (Fig. 12(a)). Thus the variance of $q_k(n)$ can be calculated using the equivalent circuit shown in Fig. 12(b) where $S_{qq}(e^{j\omega}) = S_{ee}(e^{j\omega})/|C(e^{j})|^2$ is the equivalent noise spectrum defined in the section, Power Allocation and Water-Filling Strategy. This figure shows an **analysis bank** $\{H_k(z)\}$ whose input is a noise source with effective power spectrum given by (1).

Optimization of DMT Filter Banks

In this section we discuss the optimization of filter banks used in DMT systems. The variance of the symbol $x_k(n)$ in Fig. 7(a) represents its **average power** P_k. For simplicity assume that $x_k(n)$ comes from a b_k-bit PAM constellation (Fig. 2) with equal probability for all codewords. Assume further that the noise $q_k(n)$ is Gaussian with variance $\sigma^2_{q_k}$. Then the **probability of error** in detecting $x_k(n)$ can be expressed in terms of the signal power P_k, noise variance $\sigma^2_{q_k}$, and number of bits b_k. The exact expression can be found in many references (e.g., see [14, 11, 21]). The main point is that this expression can be inverted to obtain the total power in the symbols $x_k(n)$. The result takes the form [11, 21]

$$P = \sum_{k=0}^{M-1} P_k = \sum_{k=0}^{M-1} \beta\big(\mathcal{P}_e(k), b_k\big) \times \sigma^2_{q_k} \qquad (8)$$

where the exact nature of the function $\beta(\cdot,\cdot)$ is not of immediate interest. This expression says that if the acceptable probabilities of error at the bit rates $\{b_k\}$ are $\{\mathcal{P}_e(k)\}$, then the total power P has to be at least as large as the right hand side of (8). If we try to decrease $\mathcal{P}_e(k)$ for a given bit rate, we need more power.

The crucial point to note here is that the power P can be minimized by carefully controlling the variances $\sigma^2_{q_k}$ of the noise components $q_k(n)$ at the detector inputs. Given the channel $C(z)$ and the channel noise spectrum $S_{ee}(z)$, the only freedom we have in order to control $\sigma^2_{q_k}$ is the choice of the filters $H_k(z)$ (see Fig. 12(b)). But we have to control these filters under the constraint that $\{H_k, F_m\}$ is biorthogonal.

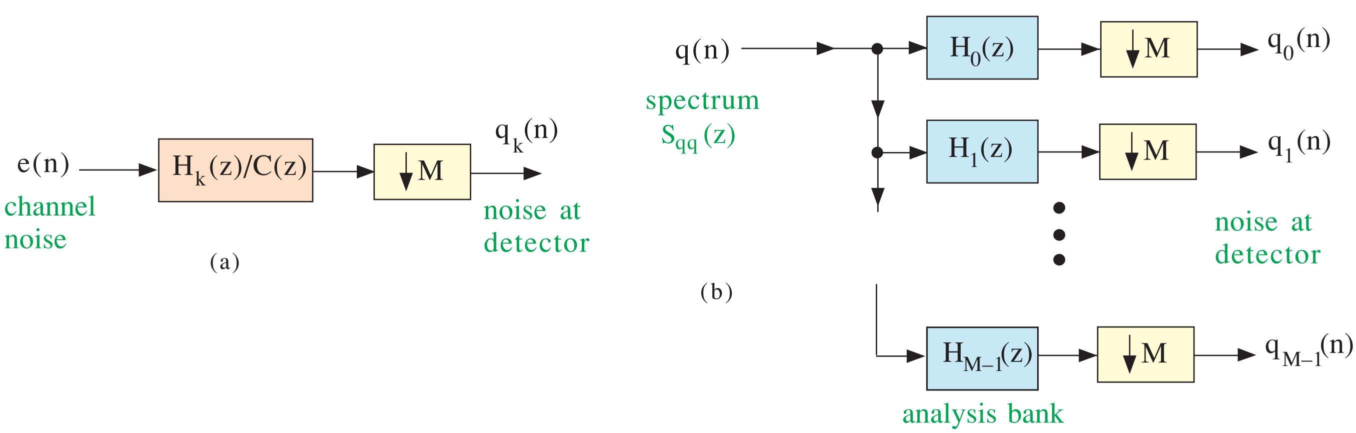


Figure 12. (a) The effect of the channel noise at the detector inputs can be modelled as the filtered version of the channel noise. (b) The noise variances at the detector inputs can therefore be calculated as the subband variances in a maximally decimated analysis filter bank, whose input has the power spectrum $S_{qq}(e^{j\omega}) = S_{ee}(e^{j\omega})/|C(e^{j\omega})|^2$.

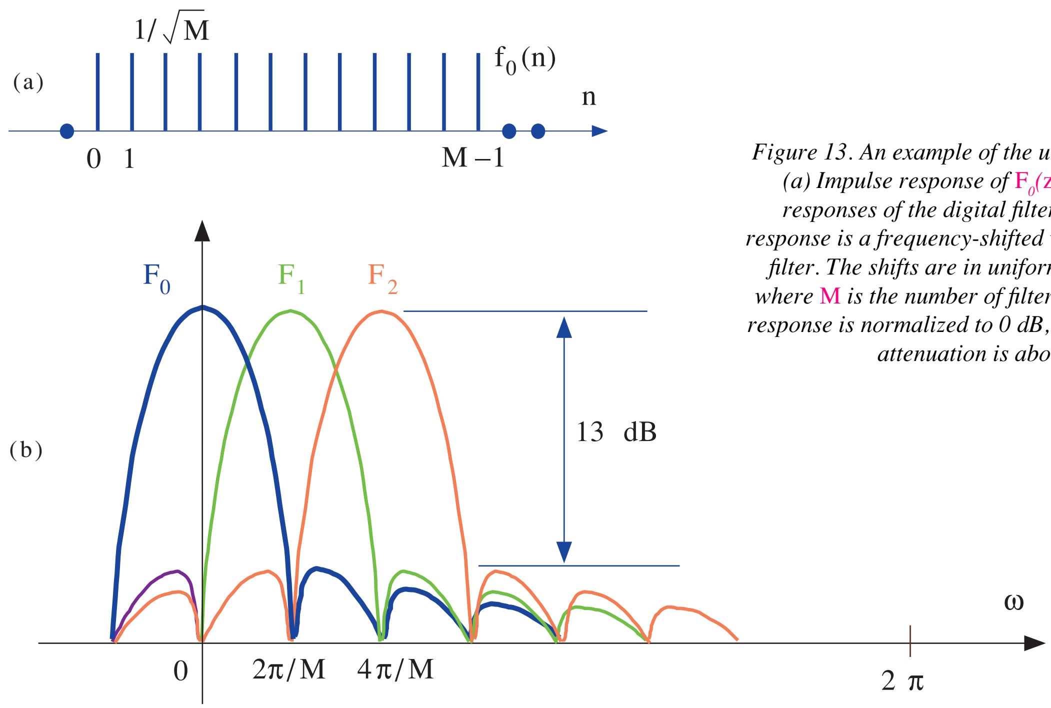


Figure 13. An example of the uniform DFT filter bank. (a) Impulse response of $F_0(z)$ and (b) magnitude responses of the digital filters $F_k(e^{j\omega})$. Each filter response is a frequency-shifted version of the preceding filter. The shifts are in uniform increments of $2\pi/M$ where M is the number of filters. If the peak passband response is normalized to 0 dB, the minimum stop band attenuation is about –13 dB.

Since the scaled system $\{\alpha_k H_k, F_m/\alpha_m\}$ is also biorthogonal (as we can show using (5)), it appears that the variances $\sigma^2_{q_k}$ can be made arbitrarily small by making α_k small. The catch is that the transmitting filters $F_m(z)/\alpha_m$ will have correspondingly larger energy which means an increase in the power actually fed into the channel. One correct approach to do the optimization would be to impose a **power constraint**. Mathematically this is trickier than constraining the powers P_k in the symbols $x_k(n)$. In the next section we confine the optimization to a class of filter banks called orthonormal filter banks. In this case the optimization problem is especially easy to formulate, and elegant solutions can be found as well.

Orthonormal DMT Systems

Recall from Fig. 7(a) that the subband channel signals $u_k(n)$ are the outputs of interpolation filters, and can be expressed as in Eq. (3). We can regard the subchannel signal $u_k(n)$ as belonging to a subspace spanned by the basis functions

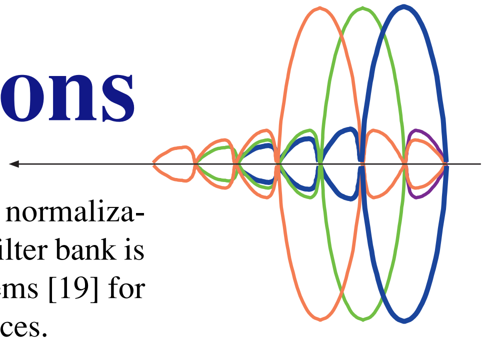
$$\ldots f_k(n+M), f_k(n), \quad f_k(n-M), f_k(n-2M) \ldots \tag{9}$$

covering the kth frequency band. The basis has an infinite number of elements, each element being a filter obtained from the preceding element by a time-shift of M samples. The composite signal $x(n)$ which enters the channel is therefore a linear combination of the basis functions from all the channels. We say that a set of M filters $\{F_k(z)\}$ is orthonormal if these basis functions are orthogonal to each other, and each of them is normalized to have unit energy. For perfect symbol recovery (or biorthogonality), the transmitting and receiving filters in any orthonormal filter bank are related by

$$h_k(n) = f_k^*(-n) \tag{10}$$

which is called **time reversed-conjugation**. This condition means in particular that the transmitting and receiving filters have identical frequency response magnitudes. Orthonormal filter banks have been extensively studied and documented, see for example [17], [20] and references therein. It is pos-

Filter Banks in Digital Communications



sible to have orthonormal filter banks where the filters are FIR. An example is the filter bank where $f_0(n)$ is chosen as a rectangular pulse of length M and $f_k(n)$ are the modulated versions

$$f_k(n) = f_0(n)e^{j\omega_k n} \qquad (11)$$

with $\omega_k = 2\pi k / M$ representing the kth center-frequency. See Fig. 13. The frequency responses are uniformly shifted versions of $F_0(e^{j\omega})$ as shown in the figure.

This is called the DFT filter bank because it can be implemented with a DFT matrix and an inverse DFT (IDFT) matrix as shown in Fig. 14. At each instant of time n, the DMT symbol $\{x_0(n), x_1(n), \ldots x_{M-1}(n)\}$ is transformed into the IDFT domain. The components $v_k(n)$ of the resulting symbol are interleaved to obtain the channel signal $x(n)$. At the receiver the signal is de-interleaved and a DFT is performed. The results $y_k(n)$ are noisy versions of the transmitted symbols $x_k(n)$. Orthonormality of the basis functions in (9) follows from the fact that the DFT matrix (with proper normalization) is unitary. The DFT filter bank is used widely in DMT systems [19] for certain types of DSL services.

The popularity of the DFT based DMT filter bank arises from the fact that if M is chosen as a power of two (e.g., $M = 512$ which is typical) the DFT can be implemented very efficiently using the fast Fourier transform (FFT) algorithm. By using bit allocation in the transform domain, the DFT based DMT system can take advantage of the shape of the effective noise spectrum (1) and obtain a performance close to the water-filling ideal (section *Power Allocation and Water-Filling Strategy*). In the *Examples* section we shall provide numerical examples in terms of bit rates and transmitted power.

Optimal Orthonormal DMT Systems

In an orthonormal DMT filter bank the transmitting and receiving filters have unit energy. So we cannot insert arbitrary scale factors in front of $H_k(z)$

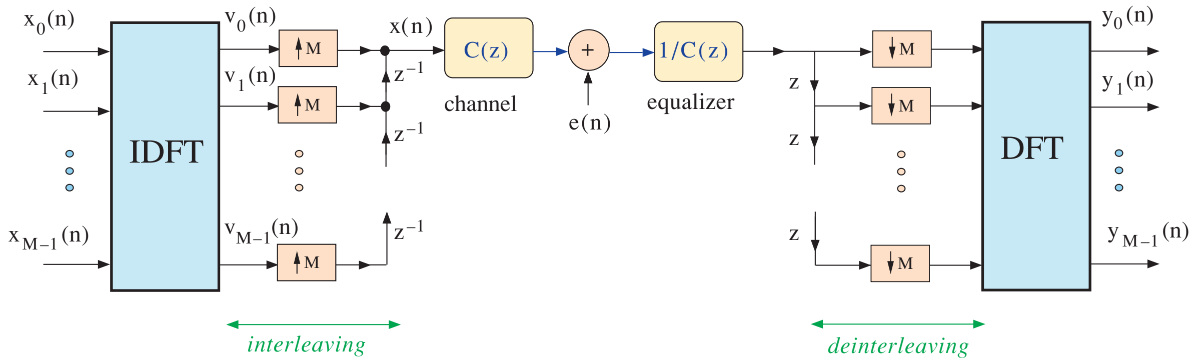


Figure 14. DMT system based on the uniform DFT filter bank. The channel equalizer 1/C(z) can be approximated well in many ways. An indirect but effective way to perform equalization is to introduce redundancies such as the cyclic prefix [22].

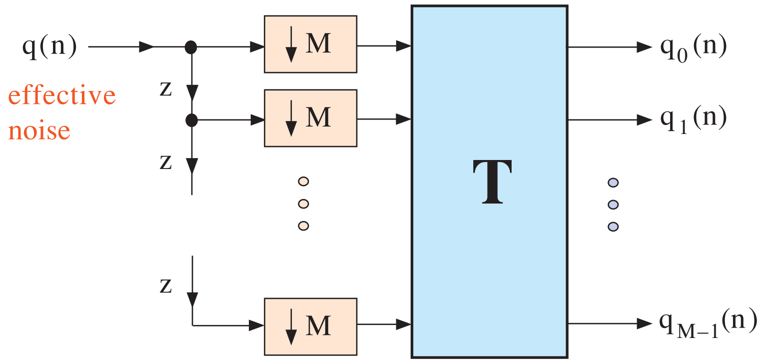


Figure 15. Noise model for the DMT filter bank, redrawn in terms of the transform matrix $\mathbf{T}$*. If* $\mathbf{T}$ *is the DFT matrix, then this is the noise model for the DFT based DMT. If* $\mathbf{T}$ *is the KLT matrix for the effective noise* q(n) *then this corresponds to an optimal DMT system. See text.*

to reduce the noise at the detector input. Moreover, orthonormality also implies that the average variance of the composite signal $x(n)$ is the average of the variances of the symbols $x_k(n)$. That is, the actual power entering the channel is proportional to the sum of powers P_k in the symbols $x_k(n)$. Refer again to Fig. 12(b) now. For a given channel the effective noise spectrum $S_{qq}(e^{j\omega})$ is fixed (ratio defined in (1)). Assume further that the integer M (number of subchannels) is fixed. For a given set of error probabilities and bit rates, the required transmitted power depends only on the noise variances $\sigma^2_{q_k}$ as shown by Eq. (8).We have to find an orthonormal filter bank such that this power is minimized. This is the problem of designing an optimal orthonormal DMT system. It turns out that the solution $\{H_k\}$ depends only on the effective noise spectrum and not on the desired values of error probabilities and bit rates.

KLT Based DMT Systems

Consider for example the class of FIR orthonormal DMT systems, that is, systems where $F_k(z)$ and $H_k(z)$ are FIR. Assume further that the filter lengths are constrained to be no larger than M. An example is the DFT based DMT system described in the section, Orthonormal DMT Systems, with transmitting filters as in (11). In view of the time-reversed conjugation property (10), the receiving filters $h_k(n)$ are given by $e^{j\omega_k n}/\sqrt{M}$ for $-(M-1) \le n \le 0$, and by 0 otherwise.

Since the channel noise is filtered by the DFT matrix, the noise model for this system can be drawn as in Fig. 15 where $\mathbf{T}$ represents the DFT matrix. This is precisely the structure of the noise model of Fig. 12(b), drawn in a different way. In general any pair of receiver noise components $q_k(n)$ and $q_m(n)$ have some statistical correlation between them. But it is possible to re-

P. P. Vaidyanathan received the B.Sc. (Hons.) degree in physics and the B.Tech. and M.Tech. degrees in radiophysics and electronics, all from the University of Calcutta, India, in 1974, 1977 and 1979, respectively, and the Ph.D degree in electrical and computer engineering from the University of California at Santa Barbara in 1982. In March 1983 he joined the Department of Electrical Engineering at the Calfornia Institute of Technology as assistant professor, and since 1993 has been professor of electrical engineering there. His main research interests are in digital signal processing, multirate systems, wavelet transforms and signal processing for digital communications.

Dr. Vaidyanathan served as vice-chairman of the technical program committee for the 1983 IEEE ISCAS, and as technical program chair for the 1992 IEEE ISCAS. He was associate editor for the *IEEE Transactions on Circuits and Systems* from 1985-1987, and is currently associate editor for the journal *IEEE Signal Processing Letters*, and consulting editor for the journal *Applied and Computational Harmonic Analysis*. He was guest editor in 1998 for special issues of the *IEEE Transactions on Signal Processing* and the *IEEE Transactions on Circuits and Systems–II*. Dr. Vaidyanathan is the author of the book *Multirate Systems and Filter Banks*. He was three times a recipient of the Award for Excellence in Teaching at the California Institute of Technology. He also received the NSF's Presidential Young Investigator award in 1986. In 1989 he received the IEEE ASSP Senior Award for his paper on multirate perfect-reconstruction filter banks. In 1990 he was recipient of the S. K. Mitra Memorial Award from the Institute of Electronics and Telecommunications Engineers, India, for his joint paper in the IETE journal. Dr. Vaidyanathan was elected Fellow of the IEEE in 1991. He received the 1995 F. E. Terman Award of the American Society for Engineering Education, sponsored by Hewlett Packard Co. In 1999 he was chosen to receive the IEEE CAS Society's Golden Jubilee Medal.

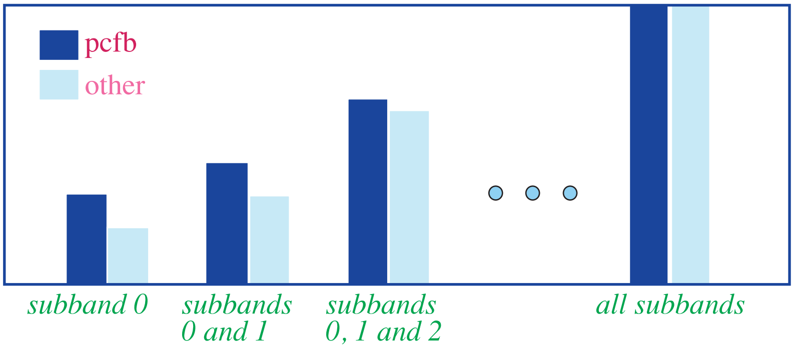


Figure 16. This figure schematically explains what a principal component filter bank (PCFB) does. The dark blue columns represent the partial sums of subband variances of a PCFB in a class $\mathcal{C}$ of orthonormal filter banks, and the light blue columns represent the same sums for an arbitrary filter bank in $\mathcal{C}$. By definition, the PCFB partial sums always dominate. Remember here that the sum of all subband variances is the same for all orthonormal filter banks, and is equal to M times the input variance.

place the DFT matrix with another unitary matrix $\mathbf{T}$ such that $q_k(n)$ and $q_m(n)$ are uncorrelated for all n when $k \neq m$. Such a decorrelating matrix $\mathbf{T}$ depends only on the power spectrum of the effective noise $q(n)$. It is called the $M \times M$ KLT matrix for $q(n)$. Essentially it is a unitary matrix which diagonalizes the $M \times M$ autocorrelation matrix of $q(n)$. It can be shown that if $\mathbf{T}$ is chosen as the KLT matrix (and its inverse used in the transmitter) then the **required power P is minimized**. The KLT offers the optimal DMT solution if we compare all orthonormal DMT systems with FIR filters of length $\leq M$. The proof follows as a special case of the results in [11, 21].

Optimal Orthonormal DMT Systems Using Unconstrained Filters

If the transmitting and receiving filters are allowed to have infinite length with no causality restrictions, then nonoverlapping brickwall filters are allowed. In fact ideal filters with multiple passbands are allowed as well and could be useful as we shall see later. Assuming orthonormality, the transmitting filters are constrained as $F_k(e^{j\omega}) = H_k^*(e^{j\omega})$. What is the best choice of the frequency responses of the receiving filters $\{H_k(z)\}$ if we wish to minimize transmitted power? The answer again depends only on the effective noise spectrum $S_{qq}(e^{j\omega})$. In fact the optimal choice of $\{H_k(z)\}$ is the so-called **principal component** filter bank or **PCFB** for the power spectrum $S_{qq}(e^{j\omega})$, as shown in [11, 21].

To explain what a PCFB is, assume that we are given a class $\mathcal{C}$ of M channel orthonormal analysis filter banks as in Fig. 12(b). Given an input power spectrum $S_{qq}(e^{j\omega})$, a PCFB in $\mathcal{C}$ is a filter bank such that the output variances $\sigma^2_{q_k}$, arranged in nonincreasing order $\sigma^2_{q_k} \geq \sigma^2_{q_{k+1}}$ have a very special property. Namely, the partial sums of these variances,

$$\sigma^2_{q_0},\quad \sigma^2_{q_0} + \sigma^2_{q_1},\quad \sigma^2_{q_0} + \sigma^2_{q_1} + \sigma^2_{q_2},\quad \ldots \tag{12}$$

are larger than the corresponding partial sums for any other filter bank in this class.[2] This idea is demonstrated in Fig. 16. If $\mathcal{C}$ is the class of orthonormal filter banks with filter length $\leq M$ then the KLT of the input is a PCFB. If $\mathcal{C}$ represents the class of ideal orthonormal filter banks (with filters allowed to be noncausal with unrestricted lengths) then there is a systematic way to construct the PCFB [21]. Unlike the brickwall filter bank of Fig. 7(c), each filter can have multiple passbands. Thus, the PCFB partitions the

> If the transmitting and receiving filters are allowed to have infinite length with no causality restrictions, then nonoverlapping brickwall filters are allowed.

[2] Readers familiar with singular value decomposition and principal component reconstruction will notice an analogy.

frequency domain in a different way according to the nature of the input spectrum.

For an arbitrary class $\mathcal{C}$ such as the class of FIR orthonormal filter banks with length constrained by some integer, the PCFB may not in general exist. The detailed theory of the PCFB is available in [23], and a tutorial review can be found in [21].

Assume that the error probabilities and total allowed power are fixed. It can then be shown that the **bit rate**, which is proportional to $\sum_k b_k$, is maximized by the PCFB. Similarly, with appropriate theoretical modelling the **information capacity** (for fixed total power) is also maximized by the PCFB. Details can be found in [24, 11, 25].

Examples

Assume that the effective noise power spectrum has the hypothetical form shown in Fig. 17(a). We have shown only the region $0 \leq \omega \leq \pi$ because we assume in this example that all time domain quantities are real valued. Assume $M = 2$ (two band DMT). The two filters of the PCFB for the above power spectrum are shown in Fig. 17(b), and the traditional brickwall filter bank response is shown in Fig. 17(d). For purpose of calculation assume that the desired probability of error is 10^{-9} in each band and that the number of bits per symbol in the two PAM constellations are $b_0 = 6$ and $b_1 = 2$. If the sampling rate is 2 MHz this implies a bit rate of 8 Mbits/sec. The average power needed can be found from (8). It turns out that the power required by the PCFB is nearly 10 times smaller than the power required by the brickwall filter bank. For example if the brickwall system requires 56 milliwatts, then the PCFB uses only about 5.67 milliwatts for the same performance! For DMT systems with larger number of bands, the difference is less dramatic. In fact for very large M the performances are nearly identical [25].

It turns out that for a monotone decreasing (or increasing) power spec-

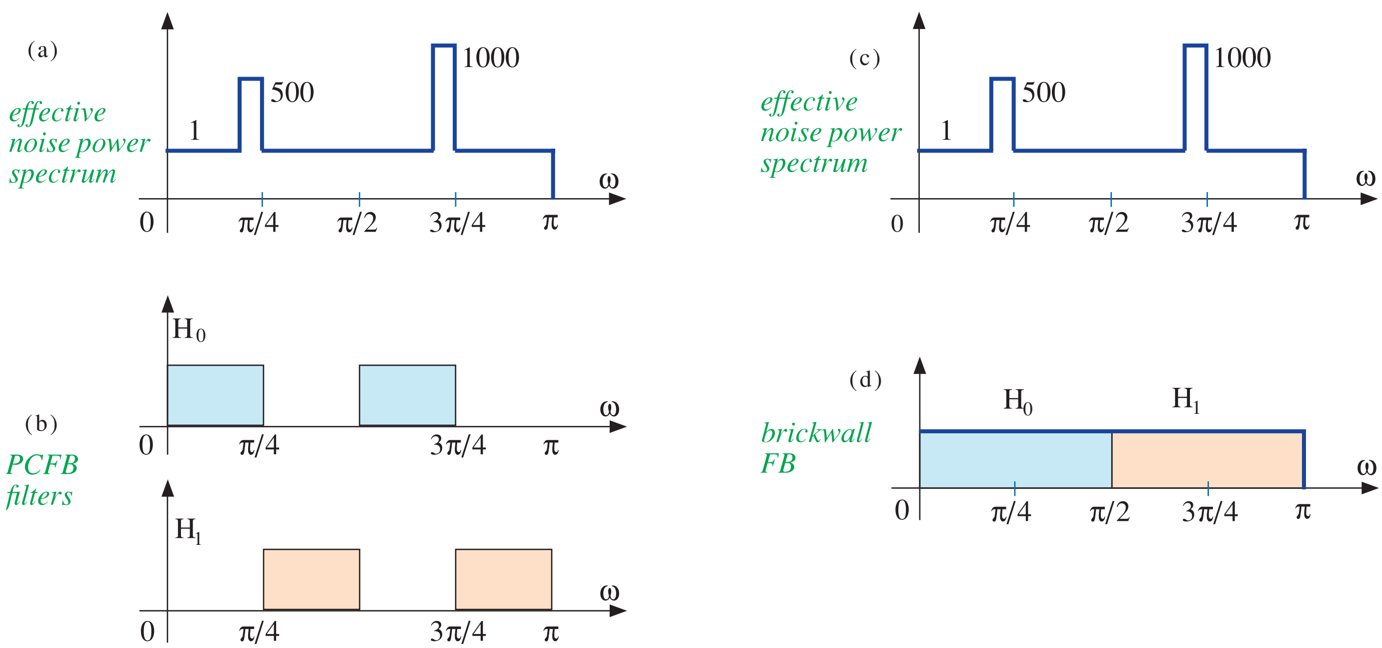


Figure 17. An example showing the difference between brickwall stacking and PCFB stacking. Here $M = 2$*. The PCFB tends to distribute the variances in such a way that one subband variance is maximized and the other is minimized. Each filter in a PCFB can have more than one passband. See text.*

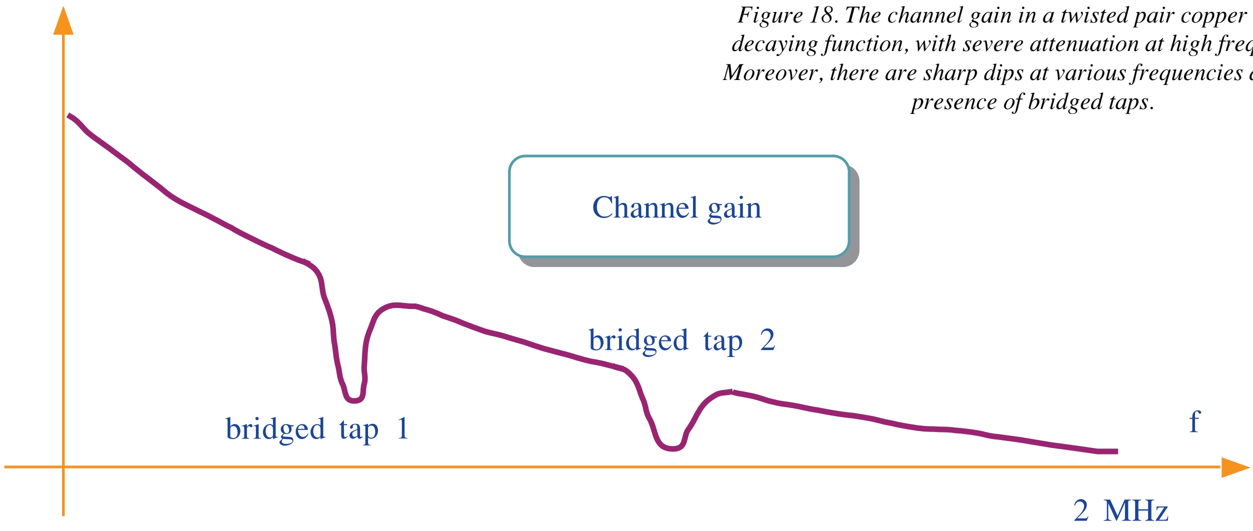


Figure 18. The channel gain in a twisted pair copper line is a decaying function, with severe attenuation at high frequencies. Moreover, there are sharp dips at various frequencies due to the presence of bridged taps.

trum the ideal PCFB is precisely the brickwall filter bank. For a power spectrum with many variations, especially bumps and dips as in Fig. 17(a) the PCFB has filters with many passbands and its performance differs significantly from the brickwall filter bank as demonstrated in the preceding example.

A practical example is the effective noise spectrum in a **twisted pair** channel used for ADSL (asymmetric DSL) service. The twisted pair is a pair of insulated copper wires that are twisted at periodic intervals.[3] It reaches every home in the world that has a wireline telephone. The channel gain of the twisted pair decays rapidly with frequency and wirelength. Figure 18 shows a typical qualitative example. The two dips in the figure are created by **bridged taps** which are used in the United States to provide additional service flexibility [2]. In spite of the large attenuation, it is still possible to use the twisted pair over a large frequency range (up to a few MHz) and achieve high rates. Several types of DSL services are based on exploiting its bandwidth like this. Originally intended for transmission of baseband speech (about 4 kHz bandwidth) more than 100 years ago, the twisted pair copper wire has therefore come a long way in terms of bandwidth utilization and commercial application. This has given rise to the popular saying that *the DSL technology turns copper into gold*.

It is typical to have 50 twisted pairs bundled into one cable for several kilofeet. As a result, the most dominant noise is the interference created by services from other cables. Two kinds of such interference can be distinguished, namely near end cross talk abbreviated as **NEXT**, and far end cross talk abbreviated as **FEXT**. Essentially, NEXT is the cross-talk from a transmitter at the same side of the cable whereas FEXT

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[3] The idea of twisting originated from Alexander Graham Bell who invented it around 1880, with a view to cancelling the effect of electromagnetic interference.

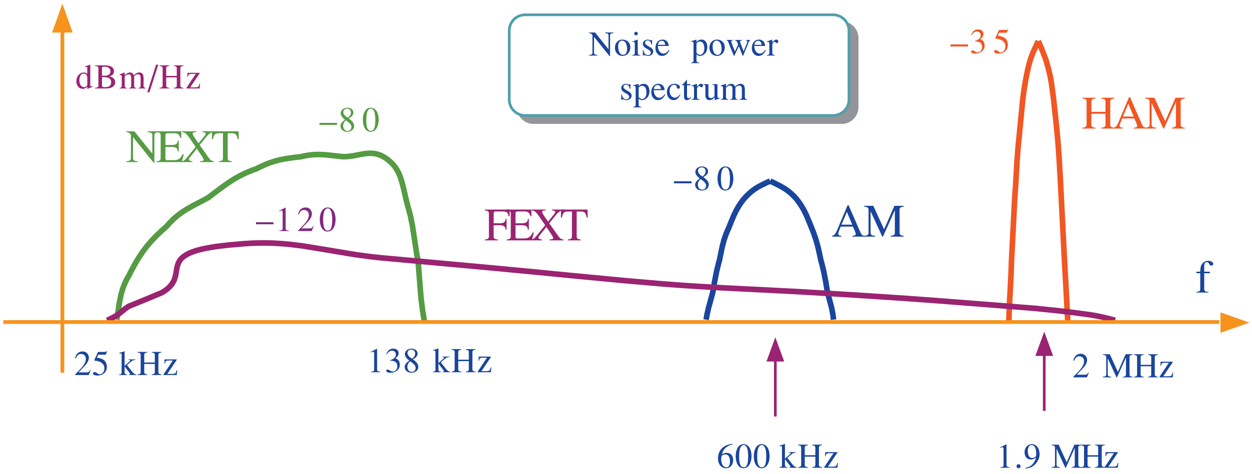


Figure 19. Various components contributing to the noise spectrum in the ADSL service offered on a twisted pair line. The figure shows the noise power spectra in milliwatts per hertz on a dB scale. The unit dBm stands for $10\log_{10}(mW)$.

is the cross-talk from a transmitter at the other end of the cable. The statistics of these have been studied for many years both theoretically and by extensive measurements [2]. Figure 19 shows typical power spectra of the NEXT and FEXT noise sources in a 50-pair cable. In addition to the NEXT and FEXT, DSL services also suffer from AM radio interference and amateur radio (HAM) interference as shown schematically in the figure. The main point of this discussion is that the total noise spectrum is quite complicated and is far from a constant or a monotone decreasing function. And since the channel gain has dips due to bridge taps, the effective noise spectrum $S_{ee}(e^{j\omega})/|C(e^{j\omega})|^2$ has several bumps and dips. A PCFB is therefore significantly different from the brickwall filter bank. A detailed example presented in [25] for typical ADSL downstream service shows that the difference in performance can be significant for a small number of subchannels M. For example, assume $M = 8$ and probability of error 10^{-9} in each subchannel. With typical numbers chosen for various noise components for the ADSL downstream scenario, the required power can be calculated. For an overall bit rate of 3.2 Mb/s it is verified in [25] that the required power is **4.68 mW for traditional DFT** type of multitone, and only **0.94 mW for**

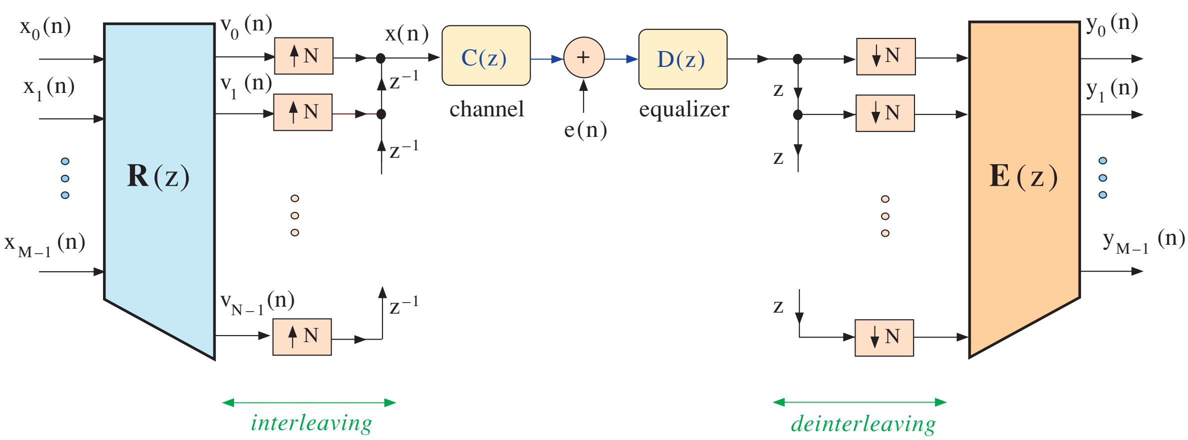


Figure 20. A DMT system with redundancy.

Filter Banks in Digital Communications

PCFB using ideal filters.The intermediate value of 2.76 mW is achieved when traditional DFT is replaced by the KLT. Finally, a traditional ideal brickwall filter bank uses 1.28 mW, slightly worse than the ideal PCFB.

Filter Banks with Redundancy

We now mention some generalizations of the DMT structure that have received significant attention recently, especially in the signal processing community. First consider Fig. 20 and outputs of $\mathbf{R}(z)$. The expanders $\uparrow N$ and the set of delay elements following them simply interleave the outputs of $\mathbf{R}(z)$ to produce the composite channel signal $x(n)$ (see Fig. 6(a)). Using standard multirate identities [17] we can draw the system of Fig. 20 in terms of transmitting and receiving filters as shown in Fig. 21. If the samples of $x_k(n)$ are separated by 1 second, for example, then the samples of $x(n)$ are separated by $1/N$ seconds, instead of $1/M$ seconds as before. This introduces

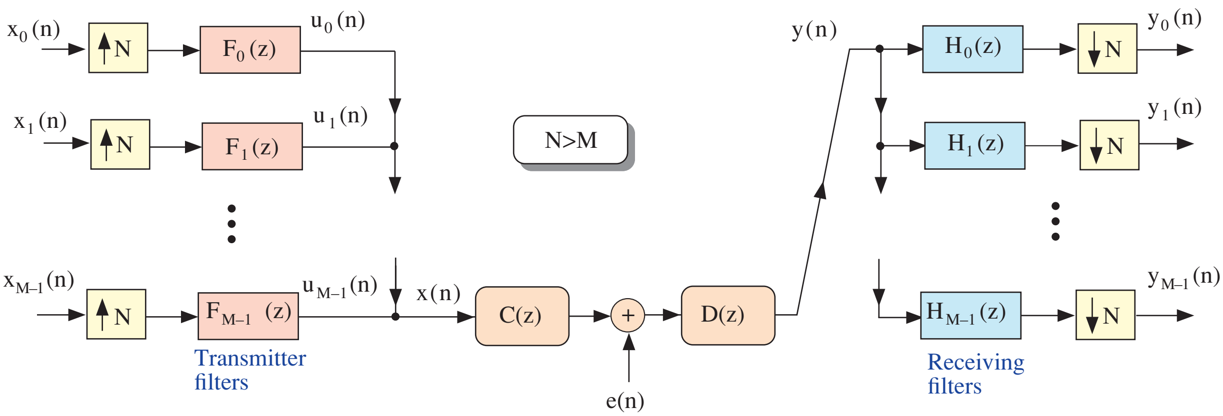


Figure 21. Redrawing the DMT system with redundancy. The only difference from Fig. 7(a) is that the expander ratio is N *which is larger than* M.

compare with the DFT based DMT system of Fig. 14. The DFT and IDFT matrices have been replaced with the matrices $\mathbf{R}(z)$ and $\mathbf{E}(z)$ which can depend on z. This means that the filters $F_k(z)$ and $H_k(z)$ can have arbitrarily large orders. This freedom can be exploited to design DMT systems with better performance (e.g., smaller total power for a given set of requirements).

Second, and more importantly, there is a new integer $N > M$ in the figure which represents the number of redundancy because the actual symbol rate of M per second has been increased to N per second. The factor N/M is called the *bandwidth expansion factor*.

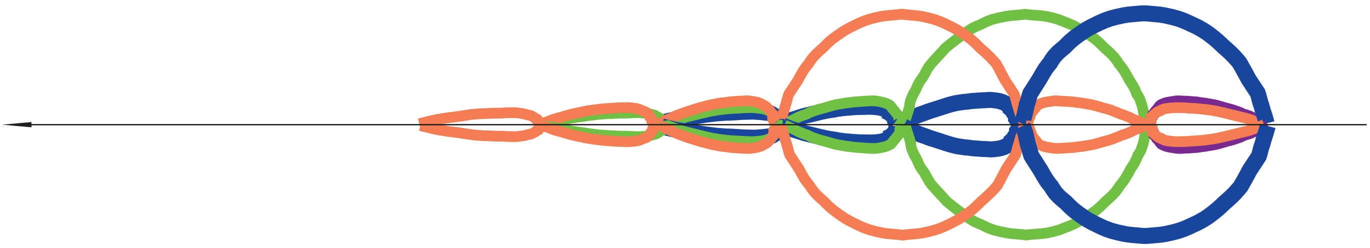
There are good practical reasons for the incorporation of such redundancy. For example channel equalization is easier [3]; there is no need to directly approximate the channel inverse $1/C(z)$, which is undesirable when $C(z)$ is a filter of high order. In a DMT system with redundancy, it is customary to use a simple FIR or IIR equalizer $D(z)$ such that the product $D(z)C(z)$ is a good approximation of an FIR filter of small length, say L. This is called the **channel shortening** step. Now, if the integer N is chosen as $N = M + L - 1$, we have $L - 1$ extra rows in the matrix $\mathbf{R}(z)$. It is possible to choose these appropriately in such a way that a simple set of M multipliers at the output of $\mathbf{E}(z)$ can equalize the channel practically completely. One special case of this idea is where the first M rows of $\mathbf{R}(z)$ are chosen from the DFT matrix and the last $L - 1$ rows are repetitions of the first $L - 1$ rows. This results in a scheme called the **cyclic prefix** explained in detail in [22]. Further interesting extensions and deeper results can be found in [26].

Filter Bank Precoders

In a DMT system the symbols $x_k(n)$ are obtained by parsing binary data $s(n)$ as shown earlier in Fig. 8(a). Instead of this, imagine that the symbols $x_k(n)$ are obtained by blocking a scalar signal $s(n)$ which itself belongs to a PAM or QAM constellation. Then the structure of Fig. 20 can be redrawn as in Fig. 22. In this system, a sequence of symbols $s(n)$ is converted to another sequence $x(n)$ before being fed into the channel.

If we assume that two successive samples of $x_k(n)$ are spaced apart by one second, then the samples of $s(n)$ are separated only by $1/M$ seconds and the channel input samples $x(n)$ are separated by the even smaller duration of $1/N$ seconds (see the blue, green and red signals in the figure). This is a way of incorporating redundancy into a signal before putting it on the channel. The system shown in the figure is called a **filter bank precoder**. By using standard multirate identities, the system of Fig. 22 can be redrawn as shown in Fig. 23(a) or equivalently as in Fig. 23(b).

There are many applications which can be described with the help of the filter bank precoder configuration. If $s(n)$ comes from a finite field and all the arithmetic operations in the filtering are finite field operations, then we can derive traditional channel coders [14] such as **block coders** and **convolutional coders** as special cases of this system. These introduce redundancy in order to make the best use of the noisy channel. A more recent application is the use of such redundancy in **channel equalization**. The channel $C(z)$ can usually be approximated well by an FIR or stable IIR filter. The zero forcing equalizer $1/C(z)$ is in general IIR and could even be unstable (poles outside the unit circle). When we introduce redundancy as above, the use of an IIR filter to approximate $1/C(z)$ is unnecessary. In a beautiful paper [7] Xia has shown that for almost any channel (FIR or IIR) there exist FIR filters $A_k(z)$ and $B_k(z)$ such that the channel is completely equalized (i.e., the received signal $r(n)$ is equal to $s(n)$ in absence of channel noise $e(n)$). In fact the well known class of fractionally spaced equalizers (FSE) [27] is a special case of the filter bank precoder with $M = 1$ and uses N-fold redundancy. The fascinating fact about the



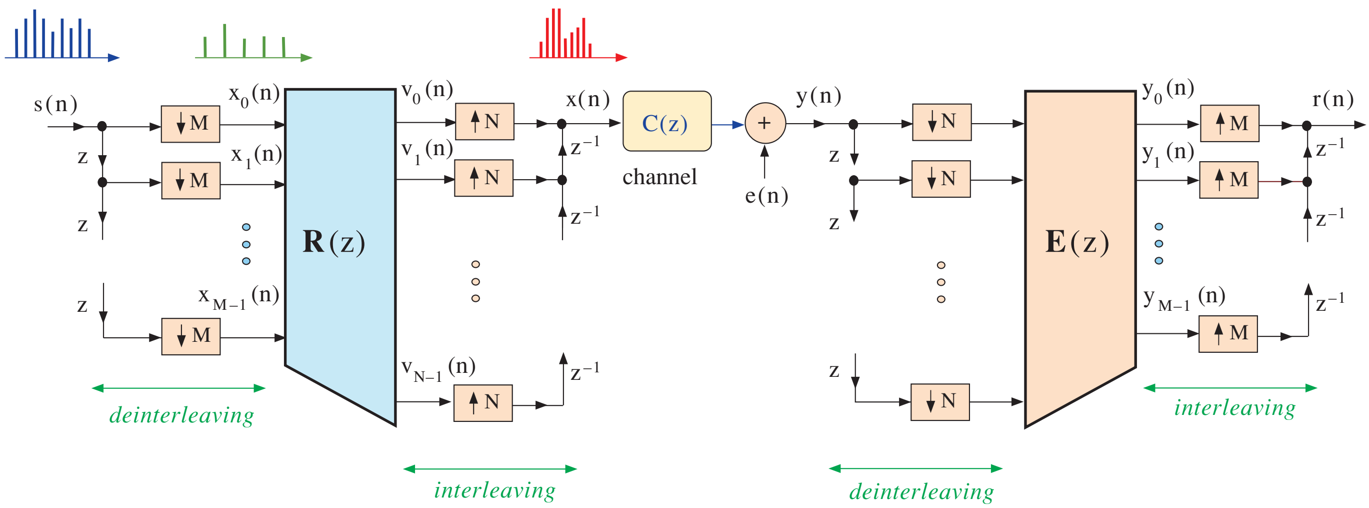


Figure 22. A modification of the redundant filter bank of Fig. 20. This is called the filter bank precoder. The only conceptual difference is in the interpretation of the vector $\{x_0(n), x_1(n), \ldots x_{M-1}(n)\}$*. The precoder allows us to equalize FIR channels with FIR filters. It also opens up the possibility of blind equalization. See text.*

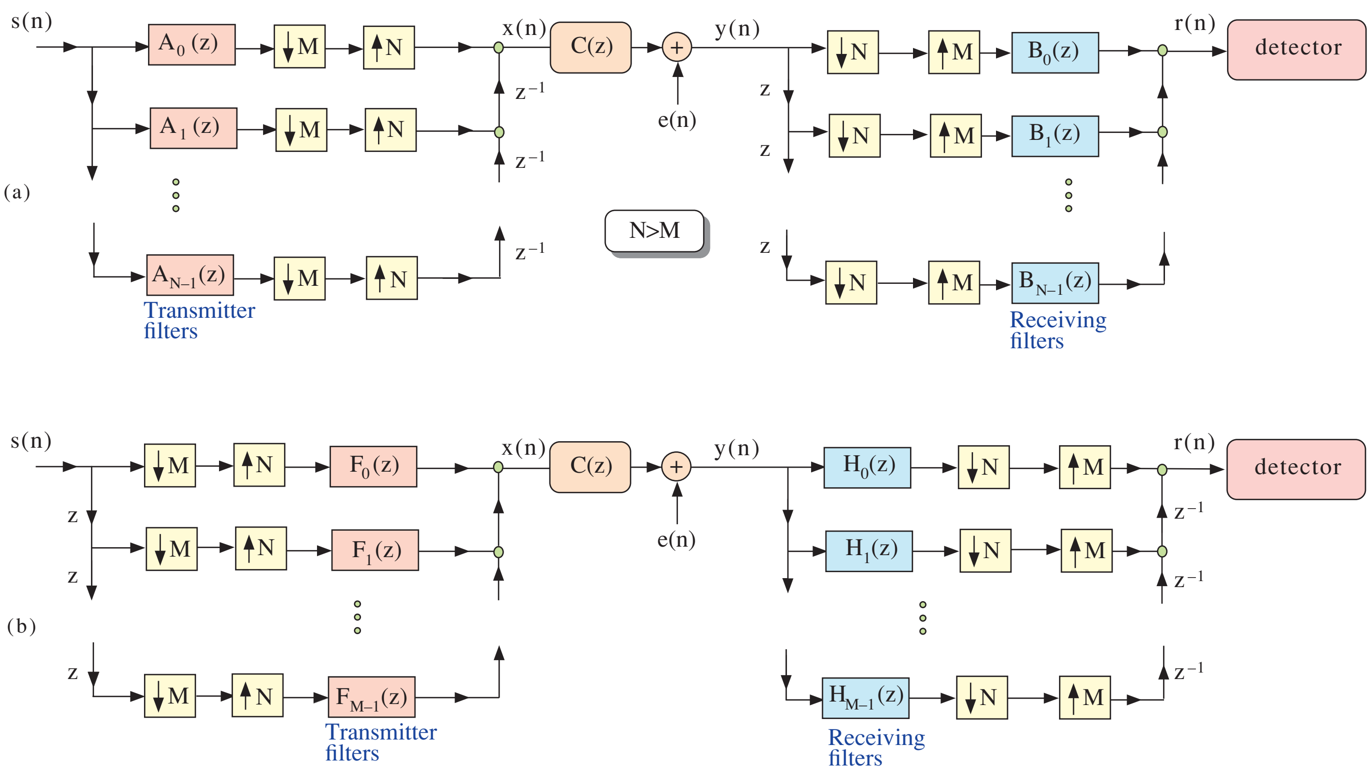


Figure 23. (a) The filter bank precoder redrawn to show the transmitting and receiving filters. Notice that there are N transmitting filters. (b) An equivalent drawing where the number of filters is M instead of N. Note that the delay and advance operators have been relocated as well. Both configurations have been used in the literature [7, 8].

filter bank precoder is that even if $M = N - 1$ it is almost always possible to have such FIR equalizers; by making N arbitrarily large we can therefore reduce the bandwidth expansion factor $N/(N-1)$ to almost unity and still have FIR equalization!

All the above discussions assume that the channel transfer function $C(z)$ is known. There are many situations where this is not true. In these cases the removal of intersymbol interference from the received signal falls under the category of **blind equalization**. It has been shown by Giannakis [12] that the redundancy introduced by filter bank precoders can actually be exploited to perform blind equalization. Further detailed results on blind as well as non-blind equalization with filter banks can be found in [8] and [13].

Concluding Remarks

Filter banks have solved a number of problems in communications, but many new questions and ideas have been opened up as well. In the section *Biorthogonality and Perfect DMT Systems*, we imposed the perfect symbol recovery condition (or biorthogonality condition) on the DMT filter bank and furthermore assumed a zero forcing equalizer. The filters were optimized under these two conditions. However, neither of these conditions is actually necessary. In fact, *a priori* imposition of these conditions is a loss of generality. It is more appropriate to optimize the transmitter and receiver filters jointly (the equalizer being regarded as part of the receiver filters). For example we could impose a power constraint and optimize these filters for maximization of signal to noise ratio at the detector input. Some of these ideas have been pursued in the context of filter bank precoders in [8]. A further generalization of the DMT system can be obtained by using nonuniform filter banks (i.e., systems where the decimator and expander are not the same in all bands).

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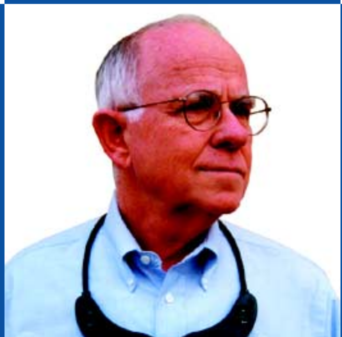
A Microphone Array for Hearing Aids



by
Bernard
Widrow

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Abstract—*A directional acoustic receiving system is constructed in the form of a necklace including an array of two or more microphones mounted on a housing supported on the chest of a user by a conducting loop encircling the user's neck. Signal processing electronics contained in the same housing receive and combine the microphone signals in such a manner as to provide an amplified output signal which emphasizes sounds of interest arriving in a direction forward of the user. The amplified output signal drives the supporting conducting loop to produce a representative magnetic field. An electroacoustic transducer including a magnetic field pick up coil for receiving the magnetic field is mounted in or on the user's ear and generates an acoustic signal representative of the sounds of interest. The microphone output signals are weighted (scaled) and combined to achieve desired spatial directivity responses. The weighting coefficients are determined by an optimization process. By bandpass filtering the weighted microphone signals, with a set of filters covering the audio frequency range, and summing the filtered signals, a receiving microphone array with a small aperture size is caused to have a directivity pattern that is essentially uniform over frequency in two or three dimensions. This method enables the design of highly-directive-hearing instruments which are comfortable, inconspicuous, and convenient to use. The array provides the user with a dramatic improvement in speech perception over existing hearing aid designs, particularly in the presence of background noise, reverberation, and feedback.*

This method enables the design of highly-directive-hearing instruments which are comfortable, inconspicuous, and convenient to use. The array provides the user with a dramatic improvement in speech perception over existing hearing aid designs, particularly in the presence of background noise, reverberation, and feedback.

Microphone Array for Hearing Aids

There is a big difference between hearing speech and understanding speech. Most hearing-impaired people will be able to hear speech when given sufficient amplification from their hearing aids. In many cases, however, they will hear but will not understand.

The benefits of amplification alone are limited. In a noisy place, hearing aids will amplify the noise as well as the desired speech signal. In a reverberant place, hearing aids will amplify late multipath arrivals as well as the direct first-arrival signal. Furthermore, feedback associated with high output hearing aids distorts the frequency response of the hearing aid, which was carefully tuned to compensate for the individual's hearing loss; and sometimes causes oscillation.

We describe a microphone array for hearing aids that overcomes some of these limitations and has the capability of enhancing speech understand-

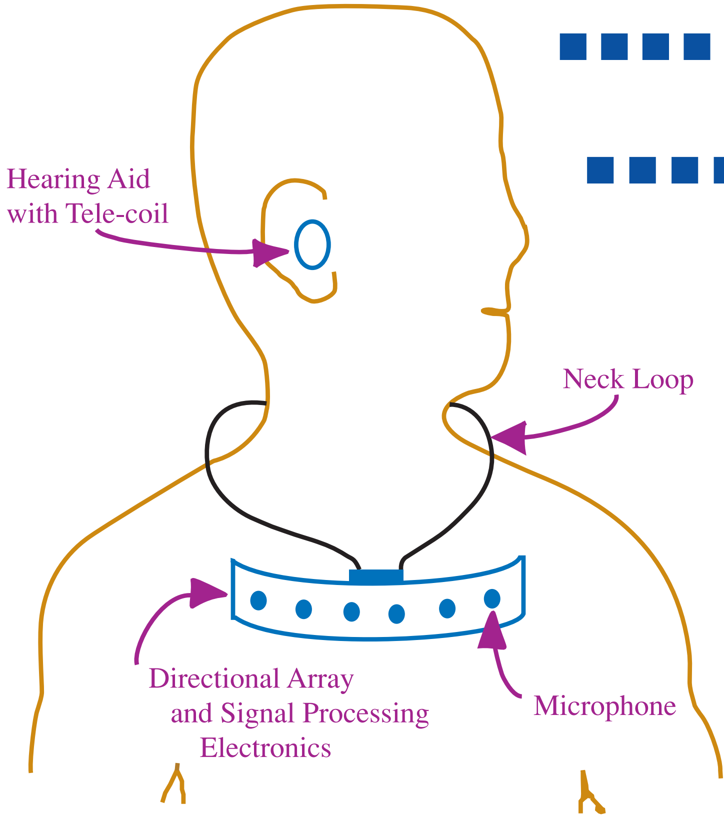


Figure 1. Chest-mounted "necklace", directional microphone array with neck loop, and hearing aid with telecoil.

ing for hearing-impaired patients. The microphone array is worn on the chest as part of a necklace, in accord with the diagram of Fig. 1. A processed signal from the array drives current through a conducting neck loop thus creating a time-variable magnetic field that is representative of the received sound. The magnetic field provides a wireless means for carrying the sound signal to conventional hearing aid devices located in the ears of the wearer. In order to receive the signal, the hearing aid must be equipped with a "telecoil", a small induction coil contained within the hearing aid whose output can be switch selected by the wearer to serve in place of the hearing aid's microphone signal. When switching the hearing aid to telecoil position, the wearer hears the sound received by the array. When switching the hearing aid to the microphone position, the wearer hears the usual sound received by the hearing aid's own microphone.

The original purpose of the telecoil was to enable the hearing aid wearer to converse over the telephone. A hearing-aid compatible telephone receiver radiates a time varying magnetic field corresponding to the telephone signal. This is generally leakage flux from the receiver. Using the telecoil, many patients can hear over the telephone much more effectively. We are able to take advantage of the telecoil, which is commonly available in the most powerful behind-the-ear hearing aid types, to provide a wireless link between the chest-mounted array and the hearing aid. Telecoils can be fitted to almost all hearing aids.

Use of the array enhances the patient's hearing in the following three ways.

Signal-to-noise ratio

The array enhances signal-to-noise ratio. The patient aims his or her body toward the person who is speaking. The array beam is 60° wide in both azimuth and elevation. The sound in the beam is enhanced relative to the surrounding sound. The speech of interest is enhanced relative to omnidirectional background noise by about 10 dB, from about 200 Hz to 6 kHz. The gains of the array sidelobes vary between 20-35 db below the gain at the center of the main beam.

Effects of reverberation

The array reduces the effects of reverberation. Because the array is gen-

A Microphone Array for Hearing Aids

erally steered toward the sound of interest, the direct primary path is thus aligned with the beam. The secondary paths for the most part arrive at angles outside the beam and are thus attenuated by the array. Reducing reverberation enhances sound clarity since the ear and the brain are somewhat confused by multiple arrivals. This is specially the case with hearing-impaired individuals.

Feedback

Use of the array reduces feedback by about 15 dB, because the chest is at a much greater distance from the hearing-aid loudspeaker than is the microphone on the hearing aid itself. Reduction of feedback makes available louder sound for the patient, without oscillation, and allows the hearing aid to function with a frequency response closer to the desired compensation curve.

The current array design and geometry are shown in Fig. 2. The device is comprised of an array of six microphones, four pushbuttons for control, and a plastic case designed to fit both the adult male and female torso. The plastic case was designed by computer, completely specified in software. It contains batteries and all of the signal processing electronics. Two custom ASIC chips were designed for this device, one for signal processing and the other to serve as an interface between a PC computer and the signal processing chip when this chip is being programmed. Custom chips were needed because of the tight space requirements and the requirements for low battery drain.

In this device, the audio spectrum from 200 Hz to 6 kHz is divided into twelve bands, each with its own digital gain control. The six microphone signals are amplified and weighted and then fed to each of the twelve bandpass filters. Different microphone-signal weightings were designed for each frequency band so that the beam width was able to be held at approximately 60° over the entire frequency range of interest. The microphone weights were designed off-line by using adaptive beamforming techniques to achieve the desired beam shape and to achieve a specified robustness to inherent variations in microphone characteristics. A least square error criterion was used for the design. Anechoic chamber testing was used to verify the de-

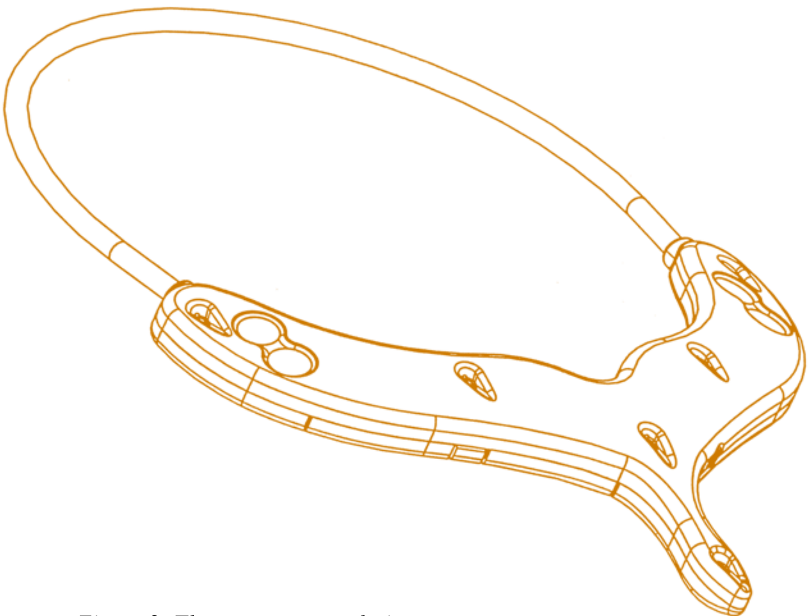


Figure 2: The current array design geometry.

sign. Theoretical and measured beam patterns turned out to be remarkably close.

U.S. Patent number 5,793,857 has been granted to Michael A. Lehr and Bernard Widrow for this technology. Canadian, European, and Australian patents have been granted, and patents are pending in other countries.

Patient testing was performed to evaluate the effectiveness of the microphone array and to compare listening with the hearing aid alone with listening to the array and hearing aid in telecoil mode. Fig. 3 shows the floor arrangement of the test room. The patient was seated before a loudspeaker that carried the sound of a male test voice. Four loudspeakers on the floor in the four corners of the room carried spectrally weighted bandpass noise. Four additional loudspeakers in the four corners at the ceiling were also used to carry the same noise. The room was not anechoic but had some sound damping. The noise carried by the eight corner loudspeakers produced a noise field that was approximately isotropic.

The test voice and the test noise were stored in a PC computer. The voice and noise data were obtained from Dr. Sig Soli of the House Ear Institute in Los Angeles. We performed a modified version of his HINT test (hearing and noise test).

With the patient seated at a prescribed location marked on the floor, the volume control of the hearing aid and the volume control of the array

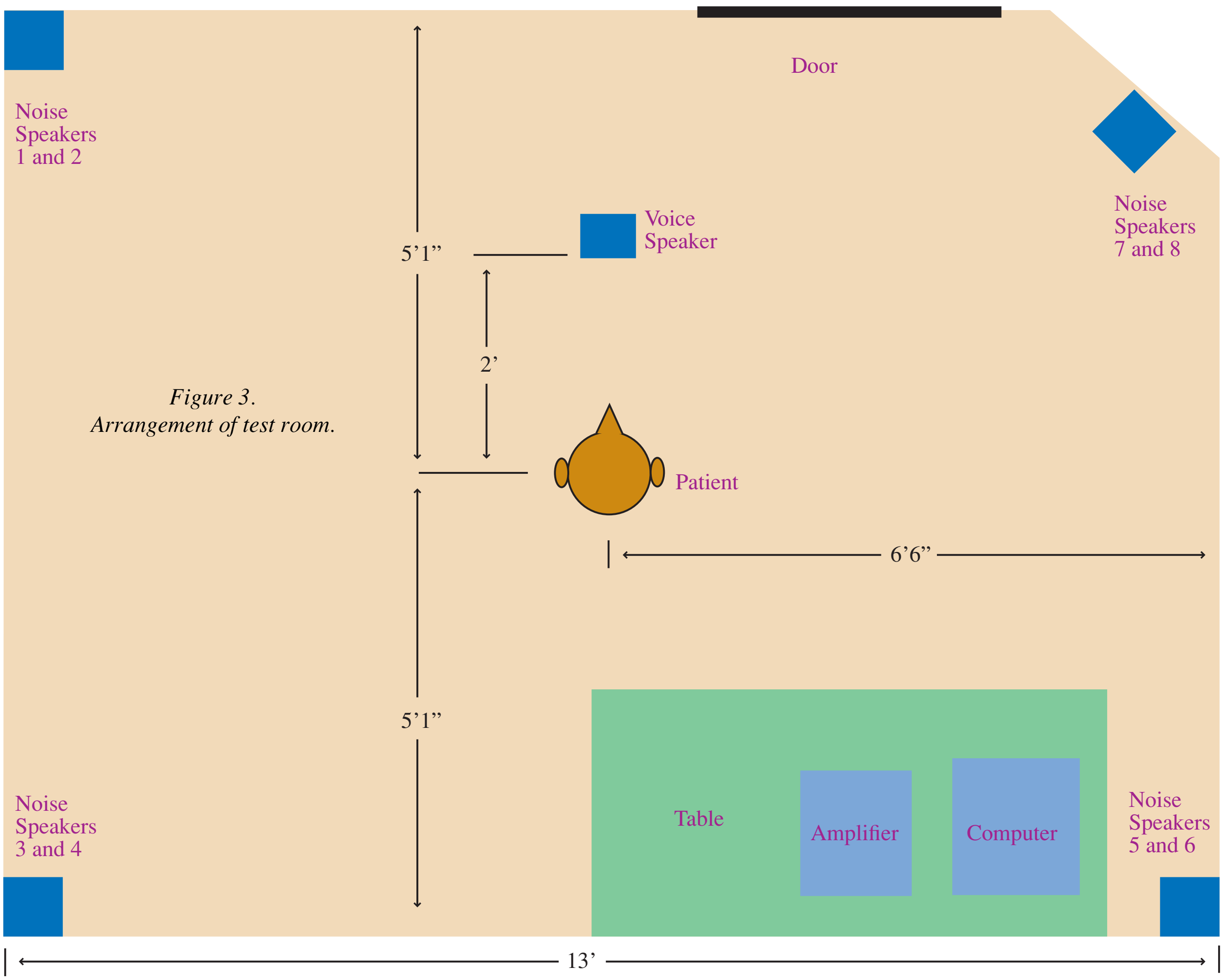
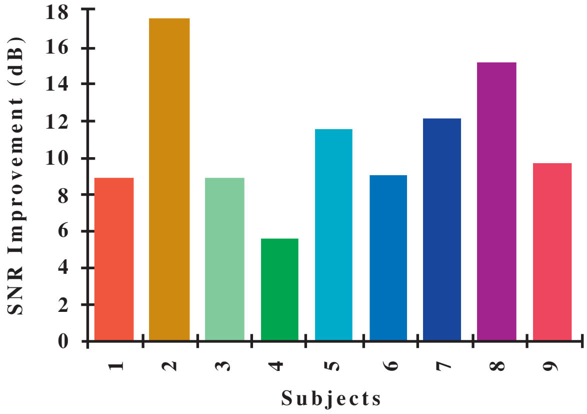
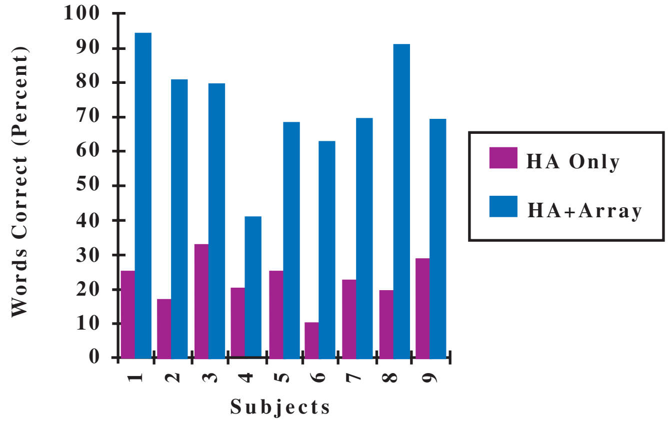


Figure 3.
Arrangement of test room.



(a)



(b)

Figure 4. Results obtained on HINT and Intelligibility tests. (a) Magnitude of improvement in sentence speech recognition threshold in noise (HINT) with the microphone array, in comparison with the hearing aid alone. (b) Percent speech intelligibility in the presence of noise. For each test subject, the purple bar is the result obtained using the hearing aid and the blue bar is the result using the array.

were set so that the measured volume delivered to the patient's ear would be the same when listening to the test voice through the hearing aid and through the array. The volume level of the test voice was set to be comfortable for the patient, in the absence of noise.

Word phrases were spoken to the patient by the test voice, with some noise applied. The patient was asked to repeat the words. If any word in the phrase was repeated incorrectly, the response was considered to be incorrect. The noise level was reduced by 2 dB, and another randomly chosen phrase was read. If the response was incorrect again, the noise was lowered by another 2 dB and so forth. When a correct response was obtained, the noise level for the next phase was raised by 2 dB. If another correct response was obtained, the noise level was raised by another 2 dB and so forth. The noise level went up and down, and the average noise level was observed over ten or twenty phrases.

The average noise level when using the hearing aid was compared to that when using the array. The improvement in signal-to-noise ratio when using the array is plotted in Fig. 4(a) for nine test patients. This improvement averages more than 10 dB, which is consistent with anechoic chamber measurements and theoretical calculations.

Other testing was done with the noise volume fixed and the volume level of the test voice fixed. Individual words randomly selected were presented by the test voice. The responses of the patients were observed when using the hearing aid, and when using the array. The results are shown for the same nine patients, in Fig. 4(b). Patient #1 had a 25% correct response with the hearing aid, and a 95% correct response with the array. Patient #2 had a 15% correct response with the hearing aid, and an 80% correct response with the array. And so forth. These improvements are rather dramatic.

One young woman in Palo Alto, California, has been wearing one of these devices on a daily basis over the past five years. As the design evolved, she always had the latest for testing. She is totally deaf in one ear and is 95–105 db below normal in her "good" ear. Using her hearing aid and with

A Microphone Array for Hearing Aids

One young woman in Palo Alto, California, has been wearing one of these devices on a daily basis over the past five years. As the design evolved, she always had the latest for testing. She is totally deaf in one ear and is 95-105 db below normal in her "good" ear. Using her hearing aid and with good lip reading, she can correctly recognize zero to two words in a typical long sentence. With her hearing aid and an array, she gets essentially every word. She can do very well even with her eyes closed. Her hearing loss is in the profound range. Hearing losses are generally characterized as mild, moderate, severe and profound. The array will find its best application with the difficult cases, the severe and profound ones.

Bernard Widrow
Stanford University
Dept. of Electrical Eng.
Packard Bldg., Rm. 273
Stanford, CA 94305
phone: (650) 723–4949
fax: (650) 723–8473
widrow@isl.stanford.edu

good lip reading, she can correctly recognize zero to two words in a typical long sentence. With her hearing aid and an array, she gets essentially every word. She can do very well even with her eyes closed. Her hearing loss is in the profound range. Hearing losses are generally characterized as mild, moderate, severe and profound. The array will find its best application with the difficult cases, the severe and profound ones.

The microphone array devices are now being manufactured and marketed by Starkey Laboratories, 6700 Washington Ave, Eden Prairie, MN, 55344, U.S.A. The trade name for the device is Radiant Beam Array (RBA). It is the most powerful hearing device on the market. It remains to be seen how well it will be accepted by the hearing-impaired community.

Bernard Widrow received the S.B., M.S. and Sc.D. degrees in electrical engineering from the Massachusetts Institute of Technology in 1951,1953, and 1956, respectively. He joined the MIT faculty and taught there from 1956–1959. In 1959, he joined the faculty of Stanford University, where he is currently Professor of Electrical Engineering.

Dr. Widrow is a Life Fellow of the IEEE and a fellow of AAAS. He received the IEEE Centennial Medal in 1984, the IEEE Alexander Graham Bell medal in 1986, the IEEE Neural Networks Pioneer Medal in 1991, the IEEE Signal Processing Society Medal in 1998, the IEEE Millennium Medal in 2000, and the Benjamin Franklin Medal of the Franklin Institute in 2001. He was inducted into the National Academy of Engineering in 1995, and into the Silicon Valley Engineering Council Hall of fame in 1999.

Dr. Widrow is a past president and currently a member of the Governing Board of the international Neural Network Society. He is associate editor of several journals, and is the author of about 100 technical papers and 15 patents. He is co-author of *Adaptive Signal Processing* and *Adaptive Inverse Control*, both Prentice Hall books. A new book, *Quantization Noise*, is in preparation.

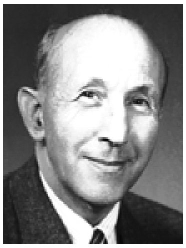
Prize Paper Awards

As noted in the ISCAS'01 report in this issue (see page 39), six best paper awards were announced at the International Symposium on Circuits and Systems in Sydney, Australia. Listed below are the awards and the papers which received them.

Guillemin-Cauer Award

"Filtering through Combination of Positive Filters Criteria"

Luca Benvenuti, Lorenzo Farina, and Brian D. O. Anderson



Ernst Guillemin

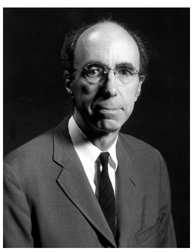
Abstract—The linear filters characterized by a state-variable realization given by matrices with nonnegative entries (called positive filters) are heavily restricted in their achievable performance. Nevertheless, such filters are the only choice when dealing with the charged coupled device MOS technology of charge routing networks (CRN'S), since nonnegativity is a consequence of the underlying physical mechanism. In order to exploit the advantages offered by this technology, the authors try to overcome the above-mentioned limitation by realizing an arbitrary transfer function as a difference of two positive filters.

IEEE Transactions on Circuits and Systems, Part I: Fundamental Theory and Applications, December 1999, pp. 1431–1440.

Darlington Award

"Voice Extraction by On-Line Signal Separation and Recovery"

Gail Erten and Fathi M. Salam



Sidney Darlington

Abstract—The paper presents a formulation and an implementation of a system for voice output extraction (VOX) in real-time and near-real-time *realistic* real-world applications. A key component includes voice-signal separation and recovery from a mixture in practical environments. The signal separation and extraction component includes several algorithmic modules with a variety of sophistication levels, which include dynamic processing neural networks in tandem with (dynamic) adaptive methods. These adaptive methods make use of optimization theory subject to the dynamic network constraints to enable practical algorithms. The underlying technology platforms used in the compiled VOX software can significantly facilitate the embedding of speech recognition into many environments. Two demonstrations are described: one is PC-based and is near-real-time, the second is digital signal processing based and is real-time. Sample results are described to quantify the performance of the overall systems.

IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing, July 1999, pp. 915–922.

Outstanding Young Author Award

"Exploiting Symmetry When Verifying Transistor-Level Circuits by Symbolic Trajectory Evaluation"

Manish Pandey (with Randal E. Bryant)

Abstract—We describe the use of symmetry for verification of transistor-level circuits by symbolic trajectory evaluation (STE). We present a new formulation of STE which allows a succinct description of symmetry properties in circuits. Symmetries in circuits are classified as *structural symmetries*, arising from similarities in circuit structure, *data symmetries*, arising from similarities in the handling of data values, and *mixed* structural-data symmetries.We use graph isomorphism testing and symbolic simulation to verify the symmetries in the original circuit. Using *conservative approximations*, we partition a circuit to expose the symmetries in its components, and construct reduced system models which can be verified efficiently. Introducing *X*-drivers into switch-level circuits simplifies the task of creating conservative approximations of switch-level circuits. Our empirical results show that exploiting symmetry with conservative approximations can allow one to verify systems several orders of magnitude larger than otherwise possible. We present results of verifying Static Random Access Memory circuits with up to 1.5 Million transistors.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, July 1999, pp. 918–935.

CSVT Transactions Best Paper Award

"On End-to-End Architecture for Transporting MPEG-4 Video over the Internet"

Dapeng Wu, Yiwei Thomas Hou, Wenwu Zhu, Hung-Ju Lee, Tihao Chiang, Ya-Qin Zhang, and H. Jonathan Chao

Abstract—With the success of the Internet and flexibility of MPEG-4, transporting MPEG-4 video over the Internet is expected to be an important component of many multimedia applications in the near future. Video applications typically have delay and loss requirements, which cannot be adequately

supported by the current Internet. Thus, it is a challenging problem to design an efficient MPEG-4 video delivery system that can maximize the perceptual quality while achieving high resource utilization. This paper addresses this problem by presenting an end-to-end architecture for transporting MPEG-4 video over the Internet. We present a framework for transporting MPEG-4 video, which includes source rate adaptation, packetization, feedback control, and error control. The main contributions of this paper are: 1) a feedback control algorithm based on Real Time Protocol (RTP) and Real Time Control Protocol (RTCP); 2) an adaptive source-encoding algorithm for MPEG-4 video which is able to adjust the output rate of MPEG-4 video to the desired rate; and 3) an efficient and robust packetization algorithm for MPEG video bit-streams at the sync layer for Internet transport. Simulation results show that our end-to-end transport architecture achieves good perceptual picture quality for MPEG-4 video under low bit-rate and varying network conditions and efficiently utilizes network resources.

IEEE Transactions on Circuits and Systems for Video Technology, September 2000, pp. 923–941.

CAD Transactions Best Paper Award

"SPFD: A New Method to Express Functional Flexibility"

Shigeru Yamashita, Hiroshi Sawada, and Akira Nagoya

Abstract—In this paper, we propose a unique way to express functional flexibility by using sets of pairs of functions called "Sets of Pairs of Functions to be Distinguished" (SPFDs) rather than traditional incompletely specified functions. This method was very naturally derived from a unique concept for distinguishing two logic functions, which we explain in detail in this paper.

The flexibility represented by an SPFD assumes that the internal logic of a node in a circuit can be freely changed. SPFDs make good use of this assumption, and they can express larger flexibility than incompletely specified functions in some cases.

Although the main subject of this paper is to explain the concept of SPFDs, we also present an efficient method for calculating the functional flexibilities by SPFDs because the concept becomes useful only if there is an efficient calculation method for it. Moreover, we present a method to use SPFDs for circuit transformation along with a proof of the correctness of the method.

We further make a comparison between SPFDs and compatible sets of permissible functions (CSPFs), which express functional flexibility by incompletely specified functions.

As an application of SPFDs, we show a method to optimize LUT (look-up table) networks and experimental results.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, August 2000, pp. 840–849.

VLSI Transactions Best Paper Award

"Toward Achieving Energy Efficiency in Presence of Deep Submicron Noise"

Rajamohana Hegde and Naresh R. Shanbhag

Abstract—Presented in this paper are 1) information-theoretic *lower bounds* on energy consumption of noisy digital gates and 2) the concept of *noise tolerance* via coding for achieving energy efficiency in the presence of noise. In particular, lower bounds on a) circuit speed f_c and supply voltage V_{dd}; b) transition activity t in presence of noise; c) dynamic energy dissipation; and d) total (dynamic and static) energy dissipation are derived. A surprising result is that in a scenario where dynamic component of power dissipation dominates, *the supply voltage for minimum energy operation* ($V_{dd,\,opt}$) *is greater than the minimum supply voltage* ($V_{dd,\,\min}$) *for reliable operation*. We then propose noise tolerance via coding to approach the lower bounds on energy dissipation. We show that the lower bounds on energy for an off-chip I/O signaling example are a factor of 24x below present day systems. A very simple Hamming code can reduce the energy consumption by a factor of 3x, while Reed-Muller (RM) codes give a 4x reduction in energy dissipation.

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, August 2000, pp. 379–391.

CALL FOR PAPERS

IEEE *TVLSI* Special SLIP Issue

The *IEEE Transactions on VLSI Systems* will publish a special issue on System Level Interconnect Prediction in the summer of 2002. This special issue focuses on system-level predictions and *a priori* and on-line (i.e., pre-layout and during layout) estimations of interconnect related design parameters and characteristics (delay, power, yield, wiring layers, ...).

It intends to build on the research work presented in the first special issue on System-Level Interconnect Prediction (*T-VLSI* December 2000) and also on work that will be presented in the second special issue (targeted for the fall of 2001). Authors are encouraged to submit high-quality research contributions that will not require major revisions. Extensions of papers presented at the IEEE/ACM International Workshop on System-Level Interconnect Prediction (SLIP 2001 http://www.SLIPonline.org) are welcomed, but work not presented at the workshop is also encouraged.

More information can be downloaded from
http://www.ece.udel.edu/~christie/Research/Slip
The submission deadline is **August 1st, 2001**.

—Phillip Christie, University of Delaware
Guest editor *TVLSI* SLIP issue

New Adventure by IEEE CAS Society

Introduction to Nanoelectronics and Gigascale Systems Technical Committee

by Chung-Yu Wu, Founding Chair
cywu@alab.ee.nctu.edu.tw

With a vast amount of research and development from high-tech industry and strong demands from personal computers, cellular phones, and Internet, the silicon semiconductor technology continues its marvelous progress into the nanometer regime in the 21st century. The great advances of semiconductor mass-production technology closely follow Moor's Law in scaling down the effective transistor channel length. It is expected that in the 130–100 nm CMOS generation for mass production in around years 2003–2006, the gate-oxide thickness will be 2 nm with the gate leakage current of 0.05 nA/μm^2, which is about 1/20 of the off-state leakage current through the transistor channel. The corresponding threshold voltage of the transistor is about 0.3 V with the power supply voltage close to 1 V. The cutoff frequency is beyond 100 GHz [1]. A significant barrier will be encountered at around the 18-nm technology node in the year 2020 as shown in Fig.1. In that technology generation, the gate-oxide thickness is below 1 nm with the gate leakage current of 0.05μA/μm^2, which is about 50 times off the off-state leakage current through the transistor channel. The threshold voltage will be below 0.1 V with the supply voltage being near 0.6 V. The transistor cutoff frequency will be beyond 500 GHz.

While the silicon semiconductor technology progresses toward the nano-scale regime, new nano-structures or nano-devices in the scale of 0.1–10 nm are under aggressive development with the possibility to supplement the capability of silicon technologies. Many innovative nano-structures/nano-devices such as resonant tunneling diodes, single-electron tunneling (SET) transistors, quantum dots, quantum wires, teraherz devices, and DNA bio-devices, have been proposed and investigated. These nano-devices and nano-structures make delicate use of quantum phenomena or interaction to perform creative physical functions.

Although technology and physics of nano-devices and nano-structures in silicon and other materials are increasingly understood, it is still a great challenge to integrate millions and billions of these devices into gigascale micro-systems. For the 18-nm technology node with BJT (bipolar junction transistor)–like gate current characteristics and 0.1-V threshold voltage, over a 1 Tera-Bit DRAM chip or logic processor chip could be built. At such an unprecedented integration level, the number of transistors on a single chip will be ten times the number of neurons in a human brain. There are many research challenges and opportunities from the circuit and system perspective to harvest the gigascale integration. Bio-inspired or neuromorphic networks might provide some stimulating information-processing architectures to alleviate severe problems of internal data transfer and the I/O function at the microchip peripheral.

Similarly, there exist great challenges in using nano-structures/nano-devices to form nanoelectronic integration systems. In nanoelectronics, quantum phenomena could be used for new signal processing operations. Electrostatic coupling or Cou-

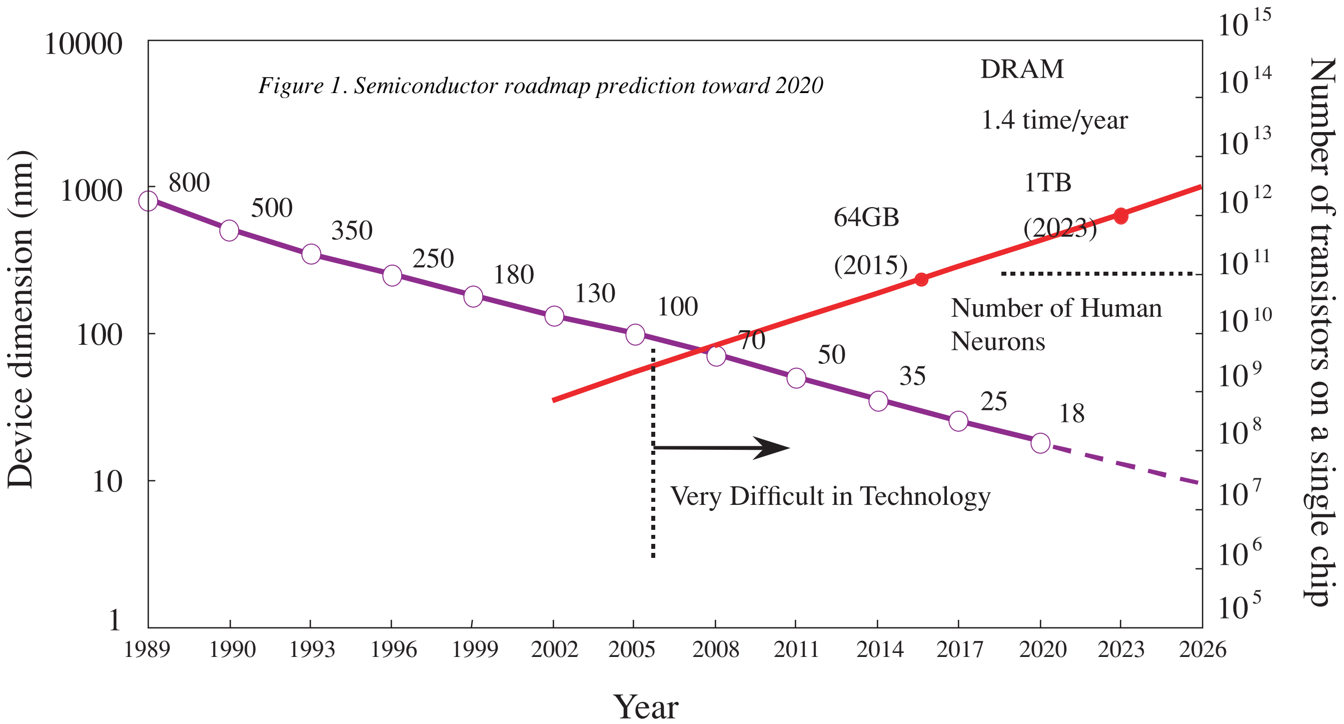
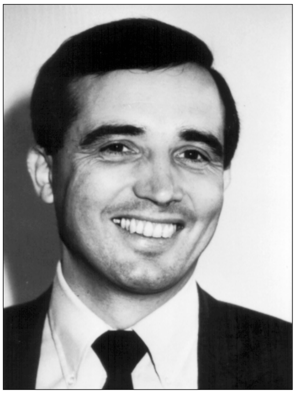


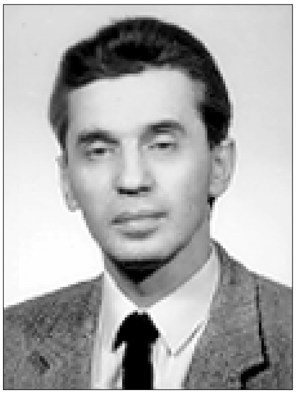
Figure 1. Semiconductor roadmap prediction toward 2020

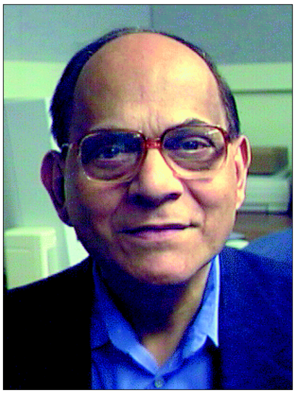

Chung-Yu Wu


Bing Sheu


Leon Chua


Josef Nossek

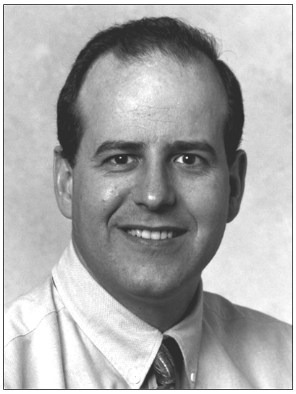

Tamas Roska


Rui de Figueiredo


Eby Friedman

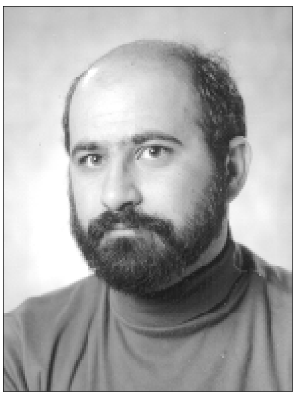

Mona Zaghloul


George Moschytz


Fathi Salam


David Chung-Laung Liu


Mohammed Ismail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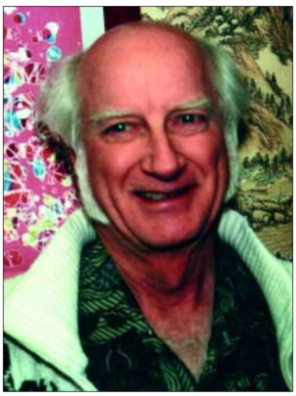

Robert Newcomb

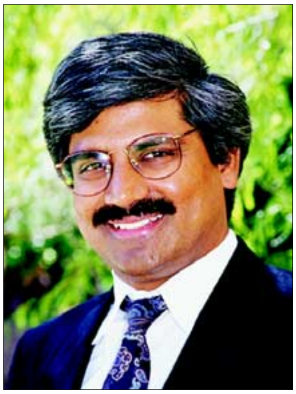

Keshab Parhi


Cliff Lau

Arpad Csurgay

Wolfgang Porod

Liang-Gee Chen



Sethuraman Panchanathan

Jeong-Taek Kong

Pedro Julian

lomb interactions could be applied for interconnection or I/O access. The promising architecture for nanoelectronic processors is quantum device or molecule arrays, such as quantum-dot cellular nonlinear networks, quantum-dot cellular automata [2], and DNA array chips. The development of nanoelectronics could lead to the applications of quantum computers, molecular computers, or DNA computers in industrial/business work and in daily life. This will bring us into a new Era in human history.

With the exciting opportunities described above, it is clear that researches on nanoelectronics and gigascale systems are tightly coupled together. To promote and excel in the areas of nanoelectronics and gigascale systems for the circuits and systems research/design community, a new technical committee was formed in the IEEE Circuits and Systems Society in early 2001. The Technical Committee on Nanoelectronics and Gigascale Systems has been actively participating in the publications, conferences, and meetings of this fast-growing profession. Active and interested researchers and engineers are all welcome.

Many enthusiastic researchers and engineers are actively involved. They include the following: Prof. Chung-Yu Wu (Technical Committee Founding Chair), National Chiao Tung University; Prof. Leon Chua (1977 President of CASS), University of California at Berkeley; Prof. Rui de Figueiredo (1998 President of CASS), University of California at Irvine; Dr. Bing Sheu (Past President of CASS), Nassda Corporation; Prof. Mona Zaghloul (VP-Technical Activities of CASS), George Washington University; Prof. George Moschytz (1999 President of CASS), Swiss Federal Institute of Technology; Prof. Josef Nossek (President-Elect of CASS), Munich University of Technology; Prof./President David Chung-Laung Liu, National Tsing Hua University, (Contributing Researcher) Prof./President Chun-Yen Chang, National Chiao Tung University; Prof. Robert Newcomb, University of Maryland; Dr. Cliff Lau, Office of Naval Research; Prof. Tamas Roska, Hungarian Academy of Sciences; Prof. Arpad Csurgay, Technical University of Budapest; Prof. Eby Friedman, University of Rochester; Prof. Fathi Salam, Michigan State University; Prof. Mohammed Ismail, Ohio State University; Prof. Andreas Andreou, John Hopkins University; Prof. Keshab Parhi, University of Minnesota; Prof. Wolfgang Porod, University of Notre Dame; Prof. Liang-Gee Chen, National Taiwan University; Prof. Ramalingam Sridhar, State University of New York at Buffalo; Prof. Sethuraman Panchanathan, Arizona State University; Dr. Jeong-Taek Kong, Samsung Electronics Co.; Dr. Pedro Julian, University of California at Berkeley. Many more will join the Technical Committee later.

References

[1] Y. Taur, "The Incredible Shrinking Transistor", *IEEE Spectrum,* vol. 36, pp. 25–29, July 1999.

[2] W. Porod, "Towards Nanoelectronics: Possible CNN Implementations Using Nanoelectronics Devices", *Proceedings of IEEE International Workshop on Cellular Neural Networks and Their Applications,* pp. 20–25, London, England, April 1998.

Chun-Yen Chang

Ramalingam Sridhar

ISCAS 2001 in Sydney – A Great Success

The 2001 IEEE International Symposium on Circuits and Systems (ISCAS) was very successfully held at the Convention Center near Darling Harbor of Sydney, Australia during May 5–9, 2001. More than one thousand and two hundred researchers, engineers, and students from the scientific/academic and industrial community gathered together and presented their newest and most exciting technical results/findings and exchanged ideas with their peers. As the historic first IEEE ISCAS conference to be held in the Southern Hemisphere, ISCAS-2001 shines like a bright star in the history of IEEE Circuits and Systems Society.

All the participants greatly enjoyed the keynote presentations that highlighted industrial contributions to the modern circuits and systems field: "*The Impact of SOC Methodologies on Circuits and Systems*" prepared by Fred Shlapak of Motorola Inc., and "*Cochlear Implants: Technology and Applications*" by John Parker of Cochlear Ltd. Barrie Gilbert of Analog Devices Inc. also prepared the material on "*Analog Design at the Millennial Crossroads*", but could not attend due to illness. One popular panel session was held on May 9 in the afternoon to address "*Successful Entrepreneurs: Generating Wealth from Circuits and Systems R&D (Not Necessarily in Silicon Valley)*". The panelists from successful start-up companies included Neil Weste of Radiata Inc., Antoni Cantoni of Atmoshpere Inc., and Chris Roberts of ResMed Corp.

A unique feature in this year's Technical Program was the Interactive Sessions that included brief oral presentations by the authors for the poster papers. It helped attract large audiences to the poster papers room. Many authors indicated strong interest in participating in similar arrangements in future ISCAS conferences. The tutorial sessions on May 6 were heavily sponsored by a special grant from the IEEE Circuits and Systems Society to allow more audience to attend the various talks. Conference general co-chairs, David Skellern of Radiata Inc. and Macquarie University, with Graham Hellestrand of VaST Systems Technology Corporation and University of New South Wales, the technical program chair Chris Toumazou of Imperial College, and their organizing committee deserve recognition for the wonderful success of the conference. This year's Society executive committee strongly supports the ISCAS conference, and the members include Hari Reddy as Society president, Josef Nossek as president-elect, Bing Sheu as past president, Ibrahim Hajj as VP-Administration, M.N.S. Swamy as VP-Publications, Mona Zaghloul as VP-Technical Activities, Geert de Veirman as VP-Conferences, plus regional VPs: Wasfy Mikhael, Anthony Davies, Juan Cousseau, and Nobuo Fujii. Great service contributions by Society administrator Barbara Wehner and her staff Tom Wehner were publicly recognized with a plaque presented by Graham Hellestrand.

The Symposium banquet on Tuesday evening was held in the new ballroom at the Convention Center. Truly considerate arrangements, warm friendship, and best services from the Symposium team deeply touched the hearts of all the participants. The awards ceremony was held before the banquet. Many awards were presented, including Society Awards, prize-paper awards, and IEEE Fellow awards. For the Society Awards, only Prof. Robert Newcomb attended the ceremony to receive the Society Education Award. The others will have to be presented in other IEEE meetings. Figure 1 shows the photo of Prof. Robert Newcomb, with Prof. Fathi Salam who is recipient of the Darlington Award for a *T—CAS II* paper, Dr. Bing Sheu who serves as the 2001 Society past president, and Prof. Chung-Yu Wu who serves as Society technical editor to the *Circuits & Devices Magazine*.

The IEEE Circuits and Systems Society continues to maintain a strong technical and financial position. The ISCAS attendees all plan on coming to Phoenix, Arizona to enjoy the warm weather and outdoor activities in May 2002.

—Chung-Yu Wu, CAS Technical Editor
Circuits & Devices Magazine
—Michael Sain, Editor-in-Chief
IEEE CAS Magazine

Figure 1. Photo taken after awards ceremony. (From left: Dr. Bing Sheu, Society past president; Prof. Robert Newcomb, recipient of Society Education Award; Prof. Fathi Salam, recipient of Darlington Award; and Chung-Yu Wu, Society technical editor to the Circuits & Devices Magazine.*)*

Swamy Assumes Publication Post

M.N.S. Swamy is serving as Vice President—Publications for the Circuits and Systems Society during the years 2001–2002.

M.N.S. Swamy is presently a research professor and the director of the Center for Signal Processing and Communications in the Department of Electrical and Computer Engineering at Concordia University, Montreal, Canada, where he served as chair of the Department of Electrical Engineering from 1970 to 1977, and dean of Engineering and Computer Science from 1977 to 1993. He has published extensively in the areas of number theory, circuits, systems and signal processing, and holds four patents. He is the co-author of two book chapters and three books, one of which has been translated into Chinese and Russian. He is the editor-in-chief of the *IEEE Transactions on Circuits and Systems—I* and associate editor of the *Fibonacci Quarterly*.

Dr. Swamy is a fellow of a number of professional societies including the IEEE, IEE (UK), and the Engineering Institute of Canada. He has served the IEEE in various capacities such as vice president of the IEEE CAS Society in 1976, program chair for the 1973 IEEE CAS Symposium, general chair for the 1984 IEEE CAS Symposium, vice-chair for the 1999 IEEE CAS Symposium, and a member of the Board of Governors. He is a co-recipient of the IEEE CAS 1986 Guillemin-Cauer Best Paper Award. Recently, he received the IEEE-CAS Society Golden Jubilee Medal, as well as the year 2000 IEEE-CAS Society Education Award in recognition of his contributions.

FREE Student Membership Promotion for 2001

Until August 1, 2001, the CAS Society is offering FREE membership in IEEE and the CAS Society for students. The only stipulations are that the student must be an active full time graduate or senior undergraduate student in an electrical/electronic engineering or computer engineering/sciences discipline, must be a first time applicant to the IEEE and CAS Society, and must have his or her application signed by a faculty member who is also an IEEE member.

This offer is NOT valid for renewals, previous student members whose membership has lapsed, recent graduates, or full IEEE/CAS members (i.e. employed in an engineering profession).

Students who meet the above requirements should download the special Student Membership Application at http://www.ieee-cas.org/html/student-promo.html, fill it out completely, provide necessary signatures and fax or mail it to:

IEEE Circuits & Systems Society
P.O. Box 265
15 West Marne Ave.
Beverly Shores, IN 46301
USA
Fax: +1 219 871 0211

Applicants should make sure that ALL information is provided completely and legibly. INCOMPLETE applications will be rejected. Students with additional questions may send an email message to cas.info@ieee-cas.org.

Terms & Limitations

- This offer is valid until 1 August 2001. Any applications received after this date will be rejected.
- This free student membership is being offered on a first-come, first-served basis until the allocated number of memberships has been exhausted.
- The IEEE CAS Society reserves the right to withdraw this offer at any time.

Trajkovic Begins Three-Year Term on Society Board

Ljiljana Trajkovic is now serving the first year of a three-year term as an elected member of the CAS Society Board of Governors. She presently serves as a member of the Conference and Regional Activities Divisions.

Ljiljana Trajkovic received the Dipl. Ing. degree in her native Yugoslavia in 1974, M.Sc. degrees in electrical engineering and computer engineering from Syracuse University in 1979 and 1981, respectively, and a Ph.D. degree in electrical engineering from UCLA in 1986. Dr. Trajkovic is currently an Associate Professor in the School of Engineering Science at Simon Fraser University, Burnaby, British Columbia, Canada. From 1995 to 1997, she was an NSF Visiting Professor in the Electrical Engineering and Computer Sciences Department at UC Berkeley. She was a Research Scientist at Bell Communications Research, Morristown, NJ from 1990 to 1997, and a Member of the Technical Staff at AT&T Bell Laboratories, Murray Hill, NJ from 1988 to 1990.

Her research interests include high-performance communication networks, computer-aided circuit analysis and design, and theory of nonlinear circuits and dynamical systems.

Dr. Trajkovic was recently elected to the IEEE Circuits and Systems Board of Governors. She is also associate editor of the *IEEE Transactions on Circuits and Systems (Part II)*. She was chair of the IEEE Technical Committee on Nonlinear Circuits and Systems (1998), and associate editor of the *IEEE Transactions on Circuits and Systems (Part I)* from 1993–1995. She also serves on various technical committees of IEEE conferences. She is the vice chair of the upcoming ISCAS 2004, to be held in Vancouver, British Columbia.

Editor's Note: Beginning with this issue, Circuits and Systems Magazine *is profiling recently elected Society officers and members of the Board of Governors. Other electees will appear in future issues.*

Circuits and Systems Society Names 2001 Awardees

Also noted in the ISCAS'01 report in this issue (see page 39), six Society awards were announced at the International Symposium on Circuits and Systems in Sydney, Australia. Listed below are the awards and the persons who received them.

M.E. Van Valkenburg Award

Alfred Fettweis

Citation: For significant, creative and innovative research contributions to circuits and systems theory and technology, and particularly to the discipline of digital signal processing.

Technical Achievement Award

Ruey-Wen Liu

Citation: For his leadership and fundamental contributions in nonlinear circuit theory and blind signal processing; and for his unceasing leadership in enhancing and sustaining the technical vibrancy of the Circuits and Systems Society.

Society Education Award

Robert W. Newcomb

Citation: For his outstanding contributions to engineering education, the publication of pioneering textbooks in circuit theory, VLSI, and control, and his classic work on Linear Multiport Synthesis, and for being a creative and inspiring teacher and researcher in the areas of circuits and systems, microelectronics, and neural systems for close to four decades.

Meritorious Service Award

Philip V. Lopresti

Citation: For providing a quarter century of outstanding and faithful leadership and service to the CAS Society.

Industrial Pioneer Award

Aart De Geus

Citation: For pioneering logic synthesis.

Chapter-of-the-Year Award

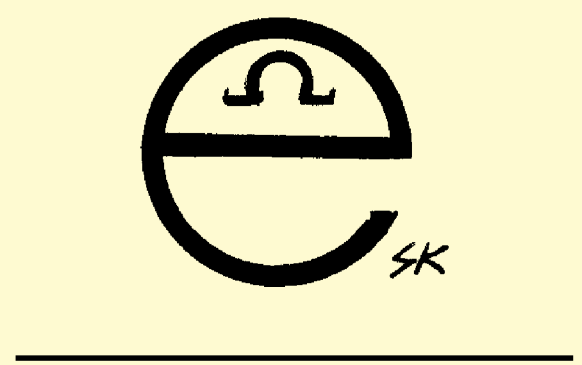
Russian CAS Chapter in Moscow

Chair: Vagan V. Shakhguildian

Vice Chair: Alexander S. Dmitriev

Justification for selection: For outstanding contributions to promoting circuits and systems related technical activities in the Moscow area as well as in other regions of the country.

THE ADVENTURES OF …
…THE 'UMBLE OHM
…Shlomo Karni



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Society Announces Divisions

President Hari C. Reddy has announced the organization of the Circuits and Systems Society into its four constituent divisions: Conference, Publications, Technical Activities, and Regional Activities. Membership and contact information follows.

Conference Division

Chair — Geert De Veirman <geert.deveirman@ti.com>
Tel: (714) 573–6829; Fax: (714) 573–6916

Ian Galton <galton@ece.ucsd.edu>
Tel: 858–822–1332; Fax: 858–822–3425

Ljiljana Trajkovic <ljilja@cs.sfu.ca>
Tel: (604) 291–3998; Fax: (604) 291–4951

Martin Hasler <martin.hasler@epfl.ch>
Tel: +41 21 693 2622; Fax: +41 21 693 6700

Peter Pirsch <pirsch@tnt.uni-hannover.de>
Tel: +49–511–762–19640; Fax: +49–511–762–19601

Georges Gielen <georges.gielen@esat.kuleuven.ac.be>
Tel: ++32–16–321047; Fax: ++32–16–321975

Ex-Officio — Hari C. Reddy <hreddy@csulb.edu>
Tel: (562) 985–5106; Fax: (562) 985–8887

Publications Division

Chair — M.N.S. Swamy <swamy@ece.concordia.ca>
Tel: (514) 848–3091; Fax: (514) 848–2802

Massoud Pedram <pedram@ceng.usc.edu>
Tel:213 740 4458; Fax:213 740 9803

Robert J. Marks <marks@ee.washington.edu>
Tel: (206) 543–6990; Fax: (206) 543–3842

Eby Friedman <friedman@ee.rochester.edu>
Tel: (716) 275–1022; Fax: (716) 275–2073

Rajesh K. Gupta <gupta@uci.edu>
Tel: 949 824 8052; Fax: 949 824 8019

Hiroto Yasuura <yasuura@c.csce.kyushu-u.ac.jp>
Tel:+81–92–583–7620; Fax:+81–92–583–1338

Chris Toumazou <c.toumazou@ic.ac.uk>
Tel: +44–171–594–6255; Fax: +44–171–581–4419

Ex-Officio — Hari C. Reddy <hreddy@csulb.edu>
Tel: (562) 985–5106; Fax: (562) 985–8887

Technical Activities Division

Chair — Mona Zaghloul <zaghloul@seas.gwu.edu>
Tel: (202) 994–3772; Fax: (202) 994–0227

Michael Green <green@ece.uci.edu>
Tel: 949 585 6854; Fax: 949 450 1079

Jason Cong <cong@cs.ucla.edu>
Tel: 310–206–2775; Fax: 310–825–2773

Ellen Yoffa <yoffa@us.ibm.com>
Tel: (914) 945–3270; Fax: (914) 945–4349

Chris Toumazou <c.toumazou@ic.ac.uk>
Tel: +44–171–594–6255; Fax: +44–171–581–4419

Andreas G. Andreou <andreou@jhu.edu>

Ex-Officio — Hari C. Reddy <hreddy@csulb.edu>
Tel: (562) 985–5106; Fax: (562) 985–8887

Regional Activities Division

Chair—Josef Nossek <nossek@nws.e-technik.tu-muenchen.de>
Tel: +49–89–2892–8501; Fax: +49–89–2892–8504

VP R1–7 — Wasfy Mikhael <wbm@ece.engr.ucf.edu>
Tel: (407) 823–3210; Fax: (407) 823–5835

VP R8 — Anthony C. Davies <tonydavies@kcl.ac.uk>
Tel: +44 20 7848 2441; Fax: +44 20 7836 4781

VP R9 — Juan Cousseau <iecousse@criba.edu.ar>
Tel: +549 155 8679; Fax: +549 155 3122

VP R10 — Nobuo Fujii <fuj@ss.titech.ac.jp>
Tel: +81 3 5734 2561; Fax: +81 3 5734 2909

Ellen Yoffa <yoffa@us.ibm.com>
Tel: (914) 945–3270; Fax: (914) 945–4349

Ljiljana Trajkovic <ljilja@cs.sfu.ca>
Tel: (604) 291–3998; Fax: (604) 291–4951

Georges Gielen <georges.gielen@esat.kuleuven.ac.be>
Tel: ++32–16–321047; Fax: ++32–16–321975

Ex-Officio — Hari C. Reddy <hreddy@csulb.edu>
Tel: (562) 985–5106; Fax: (562) 985–8887

IEEE CAS Fellow Profiles 2001

Hon-Sum Philip Wong

For contributions to solid-state image sensors and nanoscale CMOS devices.

H.-S. Philip Wong received the B.Sc. (Hons.) degree from the University of Hong Kong in 1982, the M.S. degree from the State University of New York, Stony Brook, in 1983, and the Ph.D. degree in electrical engineering from Lehigh University, Bethlehem, Pennsylvania, in 1988. He joined the IBM Thomas J. Watson Research Center, Yorktown Heights, in 1988, where he is now senior manager of exploratory devices and integration technology.

Since 1993, he has been working on the device physics, fabrication, and applications of nanoscale CMOS devices. His recent work has been on the physics and fabrication technology of double-gate and back-gate MOSFETs for CMOS technologies toward the 25 nm channel length regime.

In the applications arena, his work has been on solid-state imaging. His recent work has been imaging devices using CMOS technologies and impact of device scaling on CMOS imaging systems. His interest in solid-state imaging began when he joined IBM in 1988. From 1988 to 1992, he was a member of a team that worked on the design, fabrication, and characterization of a high resolution, high color-fidelity CCD image scanner for art work archiving. These scanners are now in use at several premier museums around the world.

Masao Hotta

For contributions to the development of low-power video-frequency analog-to-digital converters for mixed-signal system large scale integrated circuits.

Masao Hotta received the M.S. and Ph.D. degrees in electronics from Hokkaido University, Sapporo, Japan, in 1973 and 1976, respectively.

Since 1976 he has been with the Central Research Laboratory, Hitachi Ltd., Tokyo, Japan. He initially engaged in research and development of high precision monolithic D/A converters with resolution of 14 bits. From 1981 he started research and development of high-speed A/D converters for video use, and ultra-high-speed D/A converters for high definition display applications. Since 1986, he was senior researcher conducting research on analog circuits and high precision DACs and ADCs.

From 1995 to 1999, Dr. Hotta was manager of the Advanced Device Development Department, Semiconductor Technology Development Center, Semiconductor & Integrated Circuits Division, Hitachi Ltd., conducting development on microprocessors, memories, RF devices and DA/CAD systems. He is presently senior chief engineer and senior manager of the Advanced Analog Technology Center, Semiconductor & Integrated Circuits, Hitachi Ltd. He is conducting development on RF power amplifier modules, RF transceiver LSIs and mixed-signal LSIs.

Dr. Hotta served on the technical program committees of CICC, BCTM and ASIC/SOC Conferences.

Chai Wah Wu

For contributions to synchronization of chaotic systems and its applications.

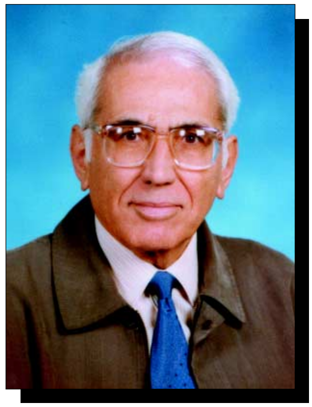
Chai Wah Wu received the B.S. in computer engineering and the B.A. in cognitive science from Lehigh University, Bethlehem, Pennsylvania in 1990, and the M.S. in electrical engineering, the M.A. in mathematics, and the Ph.D. in electrical engineering from the University of California, Berkeley in 1991, 1994 and 1995 respectively. He was a postdoctoral researcher at the University of California, Berkeley before he joined IBM T. J. Watson Research Center where he is currently research staff member in the mathematical sciences department. He has co-taught graduate level seminars on nonlinear dynamics at Columbia University and City University of New York. His research interests include synchronization in chaotic systems, digital halftoning, image watermarking and multimedia security.

Dr. Wu was associate editor of *IEEE Transactions on Circuits and Systems, Part I*. He is the author and co-author of more than 50 refereed publications and the holder of 15 US patents.

Yilmaz Tokad

For lifetime contributions to research and education in system science and circuit theory.

Dr. Yilmaz Tokad received the B.S. and M.S. degrees in electrical engineering from the Technical University of Istanbul (ITU) in 1951 and 1952. He worked for Turkish PTT as an engineer for about a year and then taught at ITU. He received the Ph.D. in electrical engineering from Michigan State University (MSU) in 1959 and served at MSU until 1971 as a professor. He continued his research and teaching activities at Middle East Technical University (METU) in Ankara and after 1974 at ITU. He was also responsible for conducting research at TUBITAK Marmara Scientific and Industrial Research Institute (MRE) where he was head of the electronics research department and then became the director of the institute. After serving seventeen years at MRE he asked for early retirement from ITU. He was at Bilkent University, Ankara (1989–1992) , and Eastern Mediterranean University at North Cyprus (1992-1997). He is now a professor at ISIK University in Istanbul. In 1982 he received the Science Award from the Turkish Scientific and Technical Research Council (TUBITAK) for his contributions in network theory. He has co-authored the book *Analysis of Discrete Physical Systems* (McGraw-Hill Book Co., 1967) and also ten books on circuits and systems, seven of them in Turkish.



Masakazu Sengoku

For contributions to graph theoretic research on circuits and communication network systems.

Masakazu Sengoku received the B.E. degree from Niigata University, Japan, in 1967, and the M.E. and Dr. Eng. degrees from Hokkaido University in 1969 and 1972, respectively. In 1972, he joined the staff at Hokkaido University as research associate. In 1978, he was associate professor in the Department of Information Engineering, Niigata University, where he is presently professor. His research interests include network theory, graph theory, transmission of information and mobile communications. He received the 1992, 1996, 1997 and 1998 Best Paper Awards from IEICE, and IEEE ICNNSP Best Paper Award in 1996. He was chair of the IEICE Technical Group on Circuits and Systems in 1995. He is a member of the editorial boards of ACM, URSI, *Wireless Networks*, and Baltzer Science Pub. He is vice-president of the Communication Society, IEICE, for 2000–2001. He is author and coauthor of more than 170 scientific publications and four books and holds several patents. He was technical program member the 51st IEEE VTC, 2000; technical program co-chair, IEEE Region 10 Conference (TENCON'99); technical program chairman, IEEE/IEICE/IEEK ITC-CSCC'99; and general vice chair, IEEE International Symposium on Multi-Dimensional Mobile Communications (MDMC'98), November 1998, among others.

Calls for Papers and Participation

IEEE-NANO 2001

First IEEE Conference on Nanotechnology

October 28–30, 2001

Outrigger Wailea Resort, Maui, Hawaii, USA

The First IEEE Conference on Nanotechnology will be held in Maui, Hawaii, USA from October 28 (Sunday) to October 30 (Tuesday), 2001. The state-of-the-art technical achievements on all aspects of nanotechnology will be reported.

IEEE/RSJ International Conference on Intelligent Robots and Systems: IROS 2001 will be held at the same place from October 29 to November 3, 2001 (http://www.icra-iros.com/iros2001).

General Co-Chairs:
Toshio Fukuda, Nagoya University, fukuda@mein.nagoya-u.ac.jp
Robert D. Shull, NIST, shull@nist.gov

Program Chair: Clifford Lau, ONR, lauc@onr.navy.mil

For more information, please check our World Wide Web site.
http://www.mein.nagoya-u.ac.jp/IEEE-NANO

2001 IEEE International Workshop on Behavioral Modeling and Simulation

BMAS 2001

October 11–12, 2001

Fountaingrove Inn — Santa Rosa, California, USA

http://www.esat.kuleuven.ac.be/~bmas

For general information, contact:
Prof. Alan Mantooth, BMAS 2001 General Chair
Department of Electrical Engineering
University of Arkansas
Fayetteville, AR 72701
E-mail: mantooth@engr.uark.edu

CALL FOR PARTICIPATION

ASIA SOUTH PACIFIC DAC DESIGN AUTOMATION CONFERENCE — A Joint Conference in 2002 — VLSI DESIGN 2002

The Seventh Asia and South Pacific Design Automation Conference
The Fifteenth International Conference on VLSI Design

January 7–11 2002, Bangalore, India

GENERAL CHAIR
Sunil D. Sherlekar
Sasken Communication Technologies Ltd, India
sds@sasken.com

For more information, please visit the website:
http://aspdac.com, or http://vlsi.ccrl.nj.nec.com, or
http://vlsidesignindia.com

ICCAD-2001

doubletree hotel san jose, ca november 4-8, 2001

International Conference on Computer Aided Design
A Conference for the EE CAD Professional

November 4–8, 2001 — Doubletree Hotel — San José, California

General Chair: **Rolf Ernst**
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Inst. Furdatenverarbeitungsanlagn
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Braunschweig D38106, Germany
49-531-391-3730; fax: 49-531-391-4587
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Conference Web site: **http://www.iccad.com**

ICME2001

IEEE International Conference on Multimedia and Expo
August 22–25, 2001 — Waseda University, Tokyo, Japan

The International Conference on Multimedia & Expo in Tokyo is the first ICME in the 21st century and the 2nd ICME co-organized by the four IEEE societies—the Circuits and Systems Society, the Computer Society, the Signal Processing Society, and the Communications Society—in joint collaboration, so as to unify all IEEE as well as non-IEEE multimedia related activities under the common umbrella of ICME.

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Waseda University
Global Information and
Telecommunication Institute, Japan
terasima@giti.waseda.ac.jp

Technical Program Chair
Jun Ohya (Waseda U./ Japan)

ICME2001 office
icme2001@giti.waseda.ac.jp

Conference Webpage
http://www.giti.waseda.ac.jp/ICME2001/

The 2002 IEEE Asia-Pacific Conference on Circuits and Systems

October 28–31, 2002 Denpasar, Bali, Indonesia

http://apccas2002.itb.ac.id
http://www.vlsi.ss.titech.ac.jp/apccas2002/

The 2002 IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS'02) is the sixth in the series of biennial Asia-Pacific Conferences sponsored by the IEEE Circuits and Systems Society.

Technical Papers Author's Schedule

Deadline for Submission of Papers:	**March 15, 2002**
Notification of Acceptance:	**June 15, 2002**
Deadline for Submission of Final Papers:	**August 15, 2002**

Please use our website above for detailed list of areas, specification of the camera-ready format and electronic submission of papers.

For further information contact Prof. Soegijardjo Soegijoko the APCCAS2002 General Chair at the Conference Secretariat, Electronics Laboratory, Department of Electrical Engineering, Institut Teknologi Bandung, Jalan Ganesha 10 Bandung 40132 INDONESIA; Tel: (62–22) 253 4117; Fax: (62–22) 250 1895; E-mail: apccas2002@ee.itb.ac.id

ISLPED'01

International Symposium on Low Power Electronics and Design
Huntington Beach, California — August 6–7, 2001

General Chair:
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enrico@athena.polito.it

Program Co-Chairs:
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vivek.de@intel.com
Mary Jane Irwin, Penn State University
mji@cse.psu.edu

ACM/IEEE ISLPED Homepage: http://www.cse.psu.edu/~islped

ASICON 2001

The 4th INTERNATIONAL CONFERENCE ON ASIC
October 22–25, 2001, Hotel Equatorial, Shanghai, China

General Co-Chairs: Qianling Zhang, Richard.M.M.Chen, Walter H.Ku

Dr. Albert Wang *(Overseas)*
3255-6 Scott Blvd
Santa Clara, CA 95054
USA
Tel: 408-327-7306
Fax: 408-986-8919
awang@tensilica.com

(P. R. China) Ms. Huihua Yu
220 Han Dan Road
Department of Electronic Engineering
Fudan University, Shanghai, 200433 P. R. China
Tel: +86-21-65643761
Fax: +86-21-65648267
hhyu@fudan.edu.cn

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2001 ICCD	S. Kundu
2001 ICECS	J. Micallef
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Transactions on Computer Aided Design of Integrated Circuits & Systems	G. De Micheli
Transactions on Circuits and Systems for Video Technology	W. Li
Transactions on Multimedia	M.-T. Sun
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Cellular Neural Networks and Array Computing	T. Roska
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Nonlinear Circuits and Systems	G. R. Chen
Power Systems and Power Electronics Circuits	A. Ioinivici
Sensors and Micromachining	M. E. Zaghloul
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** To obtain full contact information for any one of the volunteers, please contact the Society Adminstrator, Barbara Wehner at b.wehner@ieee.org.

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2002 IEEE International Symposium On Circuits and Systems

ISCAS 2002 Phoenix

MAY 26-29, 2002

http://www.iscas2002.com

Sunday, May 26, 2002 – Wednesday, May 29, 2002

Scottsdale Princess Resort Scottsdale, Arizona

ISCAS 2002 Theme:

Circuits and Systems for Ubiquitous Computing

The 2002 IEEE International Symposium on Circuits and Systems will be held in Scottsdale (Metropolitan Phoenix), Arizona on May 26–29, 2002. The Symposium is sponsored by the IEEE Circuits and Systems Society (CASS).

Authors are expected to present their paper at the Symposium. At least one author of each paper MUST register for the Symposium by January 2002 for papers to be included in the program.

Author Deadlines

Submission of Tutorial proposal	Friday, September 21, 2001
Submission of papers	Monday, October 15, 2001
Notification of paper acceptance	Friday, December 14, 2001
Author registration	Friday, January 25, 2002
Submission of FINAL paper	Monday, January 28, 2002

General Co-Chairs

Sethuraman (Panch) Panchanathan	David J. Allstot
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panch@asu.edu	allstot@ee.washington.edu

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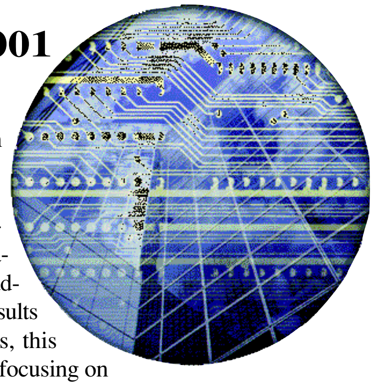
2001 Midwest Symposium on Circuits and Systems

August 14–17, 2001 Fairborn, Ohio



The Midwest Symposium on Circuits and Systems (MWSCAS) is one of the premier IEEE conferences presenting research in all aspects of theory, design, and applications of circuits and systems. In addition to presenting new research results in core circuits and systems areas, this 2001 year conference will also be focusing on innovative information technology, intelligent exploitation in microsystems and wireless information exchange. Six short courses, two plenary speakers, several invited sessions and a student paper contest are planned. Please check the symposium website for current information.

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This symposium is for researchers, practitioners, and students interested in circuits and systems, and their impact on computing, information, processing, design, and applications. This year's conference will include expanded focus on developing or using advanced aspects of theory, design, implementation, testing, and application of analog, digital, and microwave circuits and systems. Besides the general presentation session, six short courses, two plenary speakers, several invited sessions and a student paper contest are planned.

Dr. M. Ismail, Ohio State University, 205 Dreese Laboratory, 2015 Neil Avenue, Columbus, OH 43210–1272.

For further updated information, please see the symposium website.

http://www.ececs.uc.edu/~hcarter/mwscas

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